Modelling and Simulation of PI-controllers Limiters for the Dynamic Analysis of VSC-based Devices

Mohammed Ahsan Adib Murad, *Student Member, IEEE* and Federico Milano, *Fellow, IEEE*

***Abstract*—The paper discusses the modelling and the simulation of the limiters of PI controllers included in voltage-sourced converters. Seven PI controller models are considered. These include windup and anti-windup limiters, back calculation with different gains and delayed feedback and the model recommended by the IEEE standard 421.5-2016. The dynamic behavior and numerical issues arising for each PI implementation are thoroughly compared by means of a detailed all-island dynamic model of the Irish system including the HVDC East-West Interconnector and a simplified dynamic model of the Great Britain (GB) system; and the Nordic system with inclusion of a STATCOM device. Recommendations on the computer-based implementation of each model are provided in the concluding remarks.**

***Index Terms*—Proportional-integral control, anti-windup limiter, voltage-sourced converter, HVDC link, STATCOM.**

I. Introduction

A. Motivation

PI controllers are ubiquitous in power system applications, particularly in Voltage-Sourced Converter (VSC)-based devices, because of their simple structure, easy tuning and overall good dynamic performance. Since VSC-based devices often work close to their operation limits, and overcurrents can quickly damage power electronic switches, it is important to take into account and adequately model their hard limits. There are, however, several different possible implementations of PI control limiters [1], [2]. Surprisingly, different implementations can lead to substantially different dynamic responses of the system [3]. In simulations, it is also crucial to be able to distinguish between actual behaviors and numerical issues. Despite the wide spread of VSC devices, the impact of the several modeling strategies of PI controllers on the dynamic response of VSCs has received scarce attention so far. This work aims at filling this gap.

B. Literature Review

Early implementations of PI controllers were based on analog circuits with *ad hoc* anti-windup (AW) solutions [1]. Modern PI controllers are digital and employ several AW techniques, often based on the solutions used in the old analog controllers [1], [4], [5]. An overview of modern AW design and their stability properties are given in [6], [7].

The actual limiters implemented in real-world VSC controllers are often not fully known due to the non-disclosure of proprietary hardware solutions. Among all possible AW implementations of PI limiters, IEEE recommends just one model for the dynamic analysis of power systems in the standard 421.5-2016 [8]. However, the power system community as well as commercial software tools have adopted several other alternative implementations depending on the application. For example an AW technique known as back calculation type is applied in different applications [9]–[11]. References [9] and [10] consider VSC-based applications HVDC and STATCOM respectively and [11] considers an energy storage-based damping controller.

From the simulation point of view, the non-smooth behavior of the IEEE AW model poses several challenges for both software implementation and numerical integration. Known issues are the deadlock behaviour that may occur in wind turbine generators as discussed in [12], [13]; and the discretization and "algebraization" issues discussed in [14]. References [12]–[14] propose numerical techniques to alleviate the adversities of the IEEE standard model using *ad hoc* approaches. These techniques, i.e., the use of auxiliary discrete variables and the semi-implicit approach originally proposed in [15], are addressed in this paper.

C. Contributions

Based on the preliminary results given in [3], this work provides a comprehensive analysis of modelling strategies of the PI controllers included in VSC devices. In particular, the contributions of the paper are as follows.

- A complete review of the taxonomy of PI limiter models.
- A thorough discussion of the numerical issues associated with the discontinuities of anti-windup limiters.
- A detailed comparison of heuristic methods to handle numerical issues that come with the PI model proposed in the IEEE standard 421.5-2016.
- The impact of different implementations of anti-windup limiters of PI controllers on the dynamic response of VSC-based devices is thoroughly discussed.
- Recommendations on good practices on how to properly implement and utilize anti-windup limiters based on the results of several case studies that consider real-world test systems.

D. Organization

The remainder of this paper is organized as follows. Section II introduces different limiting methods of PI controllers and Section III discusses implementation and numerical issues associated with PI controllers with anti-windup limiters. Next, Section IV presents the model of the VSC, its controllers along with tuning method and shows how the limiting methods are

Mohammed Ahsan Adib Murad and Federico Milano are with the School of Electrical and Electronic Engineering, University College Dublin, Ireland. E-mail: mohammed.murad@ucdconnect.ie, federico.milano@ucd.ie.

Mohammed Ahsan Adib Murad and Federico Milano are supported by Science Foundation Ireland (SFI) under Grant No. SFI/15/IA/3074.

applied to the controllers of the VSC-based devices. Then Section V illustrates the dynamic behavior of the PI limiters of VSCs through two real world case studies: (i) a 1,479-bus dynamic model of the all-island Irish system connected to a simplified 63-bus dynamic model of the GB system through a HVDC link that represents the East-West Interconnector (EWIC); and (ii) a 74-bus dynamic model of the Nordic system with inclusion of a STATCOM device. Finally conclusions and future work are drawn in Section VI.

II. PI Controllers

The Proportional, Integral and Differential (PID) control is the most common control technique utilized in engineering applications. In power systems, the derivative component is often dropped as it can deteriorate the dynamic performance due to the presence of noise and the occurrence of large disturbance [1]. Thus this paper focuses exclusively on PI controllers.

Figure 1 shows the schemes of the PI controllers considered in the remainder of this section. These include an unconstrained standard PI model; a PI with windup limiter; the PI with conditional integrator anti-windup limiter recommended by the IEEE standard 421.5-2016; three types of PI controllers with back-calculation (or tracking anti-windup) limiters; and a PI with combined conditional and back-calculation limiter. Each model is discussed below.

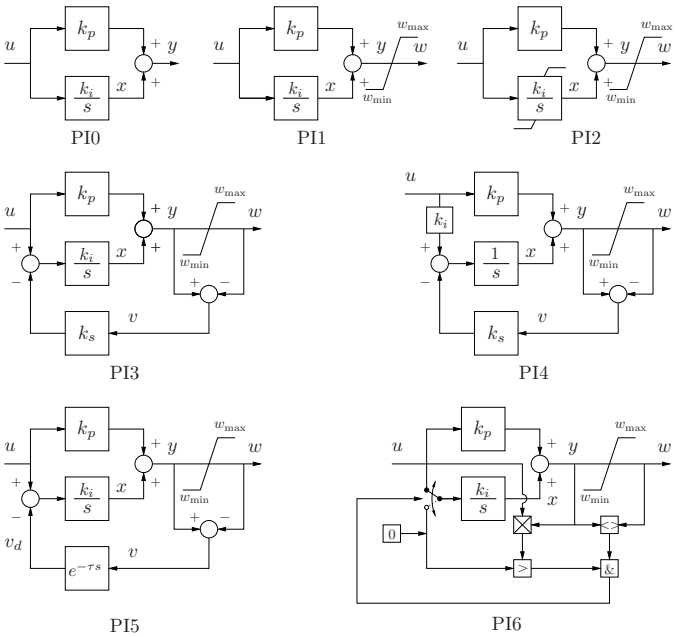

Fig. 1: PI models: (PI0) no limits; (PI1) windup limiter; (PI2) IEEE Standard 421.5-2016 with conditional integrator; (PI3) back calculation type I, (PI4) back calculation type II; (PI5) back calculation with delay; and (PI6) combined conditional and back calculation.

A. Linear Model

PI0 is the conventional model without constraints:

$$\begin{aligned} \dot{x} &= k_i u \\ y &= k_p u + x \ , \end{aligned} \tag{1}$$

where u, y, x, k_p and k_i are the input, output without limits, state variable, proportional and integral gains, respectively.

B. Windup Limiter

The PI1 model only limits the output y and thus the integral action is continuous (smooth). This model is given by (1) and:

$$w = \begin{cases} w_{\text{max}} & \text{if } y \geqslant w_{\text{max}} \ , \\ y & \text{if } w_{\text{min}} < y < w_{\text{max}} \ , \\ w_{\text{min}} & \text{if } y \leqslant w_{\text{min}} \ , \end{cases} \tag{2}$$

where w is the limited output of the controller.

C. Anti-windup Limiters

Models PI2 to PI6 include an anti-windup (AW) limiter. This paper considers the AW models commonly used in power system devices and software tools. The interested reader can find a detailed theoretical treatment of AW limiters of PI controllers in [2].

1) Conditional integrator: Conditional integration techniques consist in switching off the integration to avoid windup effects depending on certain conditions on the variables of the PI. There are several definitions of the switching conditions [4]. PI2 implements the solution proposed in IEEE Standard 421.5-2016 for power system applications, as follows [8]:

$$\begin{aligned} &\text{if } y \geqslant w_{\text{max}} : w = w_{\text{max}} \text{ and } \dot{x} = 0 \ , \\ &\text{if } y \leqslant w_{\text{min}} : w = w_{\text{min}} \text{ and } \dot{x} = 0 \ , \\ &\text{otherwise} : w = y = k_p u + x \text{ and } \dot{x} = k_i u \ . \end{aligned} \tag{3}$$

2) Back calculation: The back calculation technique consists in tracking the difference $v = y - w$ and using v as a feedback signal to compensate the input of the integrator channel of the PI when the output limits are binding. This method is also known as *tracking anti-windup* or *anti-reset windup* and can be implemented in several ways [16]. This paper considers three different tracking types. Among these, two utilize the feedback signal with gain (PI3 and PI4); and the third one implements the feedback as a pure delay (PI5).

The model of PI3 is [9]:

$$\dot{x} = k_i u - \widehat{k}_s v \ , \tag{4}$$

where $\widehat{k}_s = k_i k_s$ and k_s is the feedback gain.

The model of PI4, which is used in the software tool Simscape [17], is [12]:

$$\dot{x} = k_i u - k_s v \ , \tag{5}$$

PI5 is available in the software tool EMTP-RV [18] among several other AW techniques. The integral action is:

$$\dot{x} = k_i (u - v_d) \ , \tag{6}$$

where $v_d = v(t - \tau)$ is the delayed feedback signal and τ is the constant time delay.

3) Combined conditional and back-calculation: Model PI6 combines a conditional integration and a back calculation approach, where the summing point that performs the feedback to the integral term is replaced by a switch [4], [19]. The status of the switch depends on the following conditions:

$$\begin{aligned} &\text{if } y \neq w, \text{ and } uy > 0 \ : \dot{x} = k_i (u - v) \ , \\ &\text{otherwise} : \dot{x} = k_i u \ . \end{aligned} \tag{7}$$

III. Software Implementation and Numerical Issues

This section discusses software implementation and numerical issues arising from the PI controller models presented in Section II, as well as available techniques and modelling solutions to avoid such issues. In particular, this section discusses the *deadlock* (or *chattering*) phenomenon that occurs in model PI2 [13], [14]. Particular care is devoted to properly distinguish numerical problems due to the discretization required by computer-based integration schemes from the actual behavior of the PI controllers due to their hardware implementation.

A. Software Implementation of PI controllers

In the following, it is assumed that the numerical integration technique utilised to solve the time domain simulation is based on an implicit method, e.g., the implicit trapezoidal method (ITM) or a backward-differentiation formula (BDF) [19]. It is also assumed that the elements of the Jacobian matrix of the DAEs, say $\boldsymbol{A}_s$, are computed analytically and no symbolic refactorization is required when a limit is binding. This is obtained by describing all limits through Boolean variables and defining all elements of the sparse DAE Jacobian matrix that might be non-null in either state of such Boolean variables. This technique is relatively common in EMT simulations [20], but uncommon in transient stability analysis tools [21].

The software implementation of models PI0 to PI6 is discussed below.

- Model PI0 is linear and, thus, does not show any numerical issues, except those due to possible discontinuities and jumps of the input signal u, which are not discussed here.
- Model PI1 implements a windup limiter. This means that only the output algebraic variable w is affected by the limits. In our experience, windup limits do not lead to any numerical issue.
- Model PI2 can be implemented in various ways, some of which are known to lead to numerical issues. The numerical issue is addressed in Section III-B. A common implementation consists in introducing a discrete variable z [22] in the equation of the integrator channel of the PI:

$$\dot{x} = k_i u z \ , \tag{8}$$

  with $z = 1$ if the output of the PI controller is not saturated, and $z = 0$ otherwise. If, during the simulation, z switches from 1 to 0, x becomes constant.
- Models PI3-PI4 do not switch the dynamic state during the simulation, so it does not require to use a discrete variable and do not present numerical integration issues.
- Model PI5 uses a delay, whose integration can lead to spurious oscillations, even with A-stable integration schemes such as the ITM [23]. In our experience, however, no numerical issue arises for the typical values of the delays of model PI5 used in power system applications.
- Model PI6 is described by a set of hybrid DAEs, i.e., DAEs that mix continuous and discrete variables. It has to be noted that, in this case, discrete variables are part of the actual hardware implementation, not just a modelling issue. Physical Boolean variables, however, are treated in the same way as those introduced to emulate windup and anti-windup limits in models PI1 and PI2, respectively.

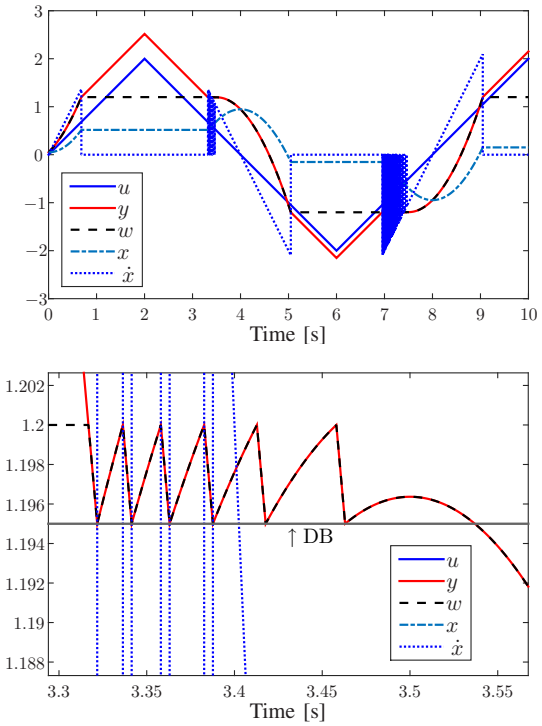

Fig. 2: Simple example to explain the deadlock phenomenon that occurs with the PI2 model.

B. Numerical Issues of the IEEE Standard 421.5-2016

We use a simple example to explain the deadlock phenomenon that can occur when using model PI2. Let assume that the following input signal is given to a model PI2:

$$\begin{aligned} \text{if } t > 2 \ \& \ \ t < 6 \text{ then: } \dot{u} &= -1 \\ \text{else: } \dot{u} &= 1 \ , \end{aligned}$$

and assume the following parameters, $w_{\max} = 1.2$, $w_{\min} = -1.2$, $k_i = 20$, $k_p = 1$ and the initial values for $t = 0$ are $x_0 = 0.05$ and $u_0 = 0$. The system is simulated for 10 s with a time step 0.001 s.

Simulation results are shown in Fig. 2. Below, we describe how a deadlock condition is reached.

- For $t < 2$ the input u to the PI controller increases. Hence, the algebraic variables of the PI, y and w, increase. Just before 1 second, $y > w_{\max} = 1.2$, w becomes constant, the integrator is locked and $\dot{x}$ switches to 0.
- For $t > 2$, u and y decrease.
- At $t = 3.317$ s, $y < 1.2$ and the integrator should unlock. However, at the very same time, $u > 0$ and, so, also $\dot{x} > 0$. Then x will increase, thus causing y to increase again towards $w_{\max}$. Depending on the time step of the integration and on the value of $\dot{x}$ and on the rate of change of the input u, a deadlock (cycling) situation can arise which consists in locking and unlocking the state variable x preventing the numerical integration to converge.

This issue cannot be removed by reducing the time step of the integration scheme and, thus, we have to conclude that the deadlock is not just a software issue. In any case, the digital hardware implementations also work with discrete quantities and are thus prone to the same issues as the numerical integration.

Three solutions to avoid the deadlock have been proposed in the literature, as follows.

- **S1:** A deadband (DB) is included into the switching logic of the integrator [12]. The DB is implemented in such a way that if the integrator is locked, it can not be unlocked unless the output w reaches the DB boundary. A similar solution discussed in [13] is based on a hysteresis, with similar properties and issues of the deadband. However, resulting equations for both approaches are same, thus we only consider the DB approach.
- **S2:** An AW on the integrator [14]. The complete model is given by the following two sets of if-then loops:

$$\begin{aligned} &\text{if } y \geqslant w_{\max} : w = w_{\max} \ , \\ &\text{if } y \leqslant w_{\min} : w = w_{\min} \ , \\ &\quad \text{otherwise} : w = y = k_p u + x \ , \text{ and} \end{aligned} \tag{9}$$

$$\begin{aligned} &\text{if } x \geqslant x_{\max} \text{ and } \dot{x} \geqslant 0 \ : x = x_{\max} \text{ and } \dot{x} = 0 \ , \\ &\text{If } x \leqslant x_{\min} \text{ and } \dot{x} \leqslant 0 \ : x = x_{\min} \text{ and } \dot{x} = 0 \ , \\ &\quad \text{otherwise} : \dot{x} = k_i u \ . \end{aligned} \tag{10}$$

- **S3:** The integrator state variable x is converted into an algebraic variable when one of the limits are binding [14].

S3 does not impose any condition on $\dot{x}$ but requires a semi-implicit formulation of the DAEs as described in [15] and, thus cannot be adopted by most power system software tools. For this reason, in the remainder of this paper, only S1 and S2 are considered. Note that using a DB of 0.005 the trajectory of the PI shown in Fig. 2 does not show a deadlock. However, the value of the DB is problem-dependent and cannot be fixed *a priori*. Further discussion on this point is provided in Section V-C1.

IV. Voltage-Sourced Converter

In recent years, the voltage-sourced converter (VSC) has become the most common AC/DC device for renewable generation, energy storage systems and HVDC connections. Both electromagnetic and averaged models has been proposed [24]. For the purpose of transient stability analysis, the Average Value Models (AVM) of electronic converters appears the most adequate [25], [26]. The AVM of the VSC along with its control, parameter tuning and constraints are presented in the remainder of this section.

A. Dynamic Model of the VSC

The configuration of a VSC is depicted in Fig. 3 which includes a transformer in the AC side, a bi-directional AC/DC converter and a condenser.

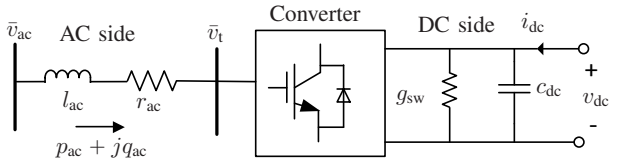

Fig. 3: VSC scheme interfacing a DC grid with an AC grid.

The dynamics of the AC side of the VSC considering a rotating dq-frame are given by:

$$\begin{aligned} r_{\text{ac}} i_{\text{ac},d} + l_{\text{ac}} \frac{di_{\text{ac},d}}{dt} &= \omega_{\text{ac}} l_{\text{ac}} i_{\text{ac},q} + v_{\text{ac},d} - v_{\text{t},d} \\ r_{\text{ac}} i_{\text{ac},q} + l_{\text{ac}} \frac{di_{\text{ac},q}}{dt} &= -\omega_{\text{ac}} l_{\text{ac}} i_{\text{ac},d} + v_{\text{ac},q} - v_{\text{t},q} \ , \end{aligned} \tag{11}$$

where $r_{\text{ac}} + jx_{\text{ac}}$ is the aggregated impedance of the converter and transformer impedances ($x_{\text{ac}} = \omega_{\text{ac}} l_{\text{ac}}$); ω_{ac}, v_{ac}, i_{ac} and v_{t} are the frequency, AC grid voltage, AC side current and AC terminal voltage, respectively. The power balance between the AC and DC sides of the converter is given by:

$$p_{\text{ac}} + v_{\text{dc}} i_{\text{dc}} - p_{\text{loss}} - \frac{1}{2} c_{\text{dc}} \frac{d(v_{\text{dc}}^2)}{dt} = 0 \ , \tag{12}$$

where $p_{\text{ac}} = (\frac{3}{2})(v_{\text{ac},d} i_{\text{ac},d} + v_{\text{ac},q} i_{\text{ac},q})$; $\frac{1}{2} c_{\text{dc}} \frac{d(v_{\text{dc}}^2)}{dt}$ is the energy variation in the capacitor; $p_{\text{loss}} = (\frac{3}{2}) r_{\text{ac}} i_{\text{ac}}^2 + g_{\text{sw}} v_{\text{dc}}^2$ are the circuit and switching losses of the converter respectively, with $i_{\text{ac}}^2 = i_{\text{ac},d}^2 + i_{\text{ac},q}^2$ and g_{sw} is obtained from a given constant conductance g_0 and the quadratic ratio of the actual current to the nominal one, as follows [27]:

$$g_{\text{sw}} = g_0 \left(\frac{i_{\text{dc}}}{i_{\text{dc}}^{\text{nom}}} \right)^2 \ . \tag{13}$$

In the equations above, AC quantities are expressed in the dq-reference frame, achieved through a Phase-Locked Loop (PLL). The PLL forces the angle of the dq-frame to track the angle θ_{ac}.

B. VSC Control

Figure 4 shows the vector-current control considered in this paper. This control strategy uses a dq-composition with the grid voltage as phase reference, an inner current control loop to decouple the current into its d and q components, an outer control loop utilizes the d component to control active power or DC voltage, and the q component to control reactive power or AC voltage. Both inner and outer loops are implemented with PI controllers [28], [29].

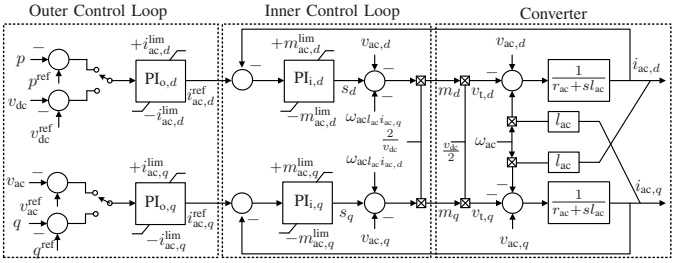

Fig. 4: VSC converter, outer control and inner current control in dq-frame.

C. Current Limiters

Active and reactive power transfer capabilities are always constrained in VSC-based devices. Violations of the operating limits can occur following a large disturbances such as a fault or a line outage. Protections strategies aim at recovering VSC currents to the pre-fault steady state. Depending on the power-electronic interface, commonly found protection mechanisms include [30]: (i) ac-side over-current limiting; (ii) modulation index limiting; (iii) reactive current boosting during faults; and (iv) fault-ride-through during ac faults.

The advantage of using the control structure described in Section IV-B is that it can limit the current flowing into the converter during the disturbances. In the implemented model of the VSC, such current limitation strategy is achieved through the PI controllers of the outer loop. Current limit values are chosen based on the priority between active (p) and reactive (q) power depending on the applications.

If the priority is given to the active power, $i_{\mathrm{ac},d}^{\mathrm{ref}}$ is limited to the maximum current capacity $\pm i_{\max}$ whereas $i_{\mathrm{ac},q}^{\mathrm{ref}}$ is limited in such a way that the total current does not exceed the maximum current rating of the converters, as follows:

$$\begin{aligned} i_{\mathrm{ac},d}^{\max} &= i_{\max} \\ i_{\mathrm{ac},q}^{\max} &= \sqrt{i_{\max}^2 - i_{\mathrm{ac},d}^2}\ . \end{aligned} \tag{14}$$

D. Controller Tuning

The tuning of the PI controllers is carried out considering the closed-loop dynamic response of the system when the PI control is *not* limited. In practice, PI controllers are first designed without explicitly considering saturation constraints. Then an anti-windup limiter is applied to reduce the windup effect [1], [31]. Since the model of a non-saturated PI controller is unique, the first step will always result in same proportional and integral gain parameters for all the PI models considered in the paper.

The structure of the controllers for both d- and q-axis current control loops are identical and so are assumed to be their parameters. The gains for the PI controllers in the inner control are chosen based on the pole cancellation technique as follows [26],

$$k_p = \frac{l_{\mathrm{ac}}}{\tau_c}\ , \qquad k_i = \frac{r_{\mathrm{ac}}}{\tau_c}\ , \tag{15}$$

where τ_c is the desired time constant of the closed loop step response, the typical range of τ_c for VSC-based applications is $[0.5, 5]$ ms [32]. We have used a trial-and-error technique for the tuning of the outer controllers and the back calculation gains for PI3 and PI4. However feedback gains in PI3 and PI4 can be can be tuned using other techniques, i.e., a Linear Matrix Inequality (LMI) technique such as the one discussed in [6].

V. Case Study

In this section, two applications of VSC-based devices are dicussed: (i) point to point VSC-HVDC link (Section V-B); and (ii) a STATCOM device (Section V-C). The case study of VSC-HVDC link considers converter limits without grid operational limits; whereas the case study on the STATCOM considers grid operational limits along with converter limits.

A. Software tool

The Python-based software tool DOME [21] is used to solve all simulations.

1) Implementation method: DOME implements a fixed-structure DAE. This means that if-then rules of the anti-windup limiters are converted first into discrete variables that can take only 1 or 0 values and then these variables are utilized to multiply the part of the equations and the elements of the Jacobian matrices that are relevant to the limiter. Detail of such implementation is described in [22]. In this way, Jacobian matrices have always the same non-zero elements (even is, incidentally some of these elements are actually null) and are symbolically factorized only once, at the beginning of the simulation, and numerically factorized only whenever a discrete variable changes its value (i.e., a limiter or any other discrete event "jumps").

2) Simulation setup: DOME allows choosing different solvers (implicit trapezoidal methods, backward differentiation formulas of various orders, backward Euler, etc.) and a variety of factorization methods and adaptive step size approaches. We have tested all PI limiter models with the solvers above and with different setups and always found consistent results. We can thus reasonably exclude that the issues discussed in the paper are due to the solver. Unless stated otherwise, the simulations are solved using implicit trapezoidal integration method with 1 ms fixed time step.

B. Case Study 1: VSC-HVDC Link

This case study considers the all-island Irish transmission system connected through the VSC-HVDC link, namely, the East-West Interconnector (EWIC), to the GB grid. The Irish network is built based on the static data provided by the Irish transmission system operator, EirGrid Group, and the dynamic data defined based on power plant capacities and technologies [33]. The system consists of 1,479 buses, 1,851 transmission lines and transformers, 245 loads, 22 Synchronous Generators (SGs) with Automatic Voltage Regulators (AVRs) and Turbine Governors (TGs), 6 Power System Stabilizers (PSSs), 173 wind generators of which 139 are doubly-fed induction generators (DFIGs) and 34 with constant speed wind turbine. The GB grid is based on [34] and consists of 63 buses (29 high voltage buses, 33 generator buses, 1 HVDC link), 98 transmission lines, 30 synchronous generators with AVRs and TGs (28 thermal, 2 hydro), 3 DFIGs, 29 loads.

1) Simulation results: The initial operating condition assumes that 450 MW are imported from the GB system to the Irish grid through the EWIC, which is modelled as a symmetric monopole-type VSC as described in [35]. The VSC controller limits on both sides of the EWIC are imposed based on converter rating and priority is given to active power.

The contingency consists of a three phase fault occurring at 0.2 s, cleared after 60 ms and located near to VSC on the Irish side of the EWIC. During the fault, both the AC voltage and active power controllers of the VSC on the Irish side reach their limits. The responses of the outer controller states, outputs and reactive powers provided by the VSC for different PI controllers are shown in Figs. 5-9. The response of

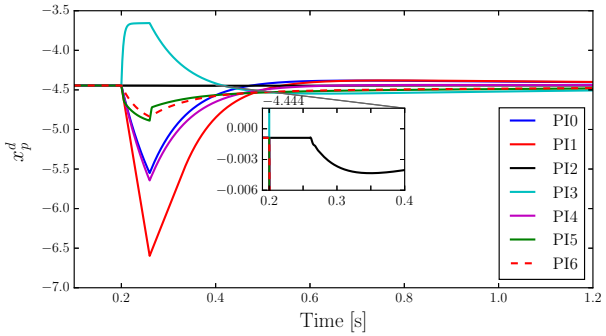

Fig. 5: Response of the integrator state (x_p^d) of the active power controller of the Irish-side VSC.

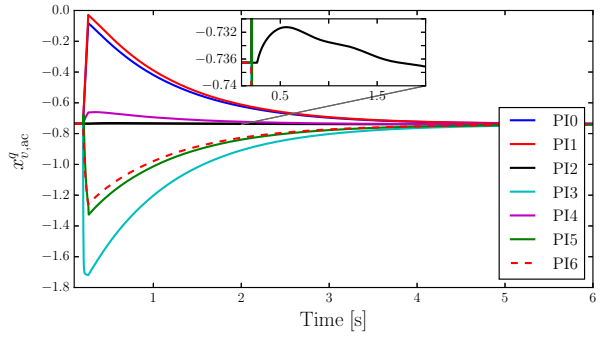

Fig. 6: Response of the integrator state ($x_{v,\mathrm{ac}}^q$) of the AC voltage controller of the Irish-side VSC.

model PI0 is included for reference to show the behavior of the system when no limits are included. Simulation results clearly show that different PI limiter models lead to considerably different transient behaviors. Relevant remarks on each PI model are given below.

The windup limiter of PI1 does not lock the integral variable x when the limits are binding, which results in a slower recovery to the control mode after the disturbance. This poor performance is typical of windup limiters, which are thus not to be recommended.

The AW limiter of model PI2 locks the integrator state variable as soon as the PI limits are binding as shown in the zoom in Figs. 5 and 6. The response of model PI2 is thus faster than that of all other PI models.

For the back calculation models PI3 to PI6, the integral term of the controller is recomputed through a feedback signal and reset to a new value so that it prevents the integrator from winding up. As the disturbance lasts 60 ms and is cleared before the integrator settles to a new value (see Figs. 5-6), back calculation methods show different responses (see Figs. 7-8) compared to model PI2, also with respect to the active and reactive power supports (the trajectory of the reactive power is shown in Fig. 9).

Finally, both models PI3 and PI4 include a feedback gain. If same gain values are used, due to their different implementations, namely (4) and (5), the two models show a different behavior. Special care, thus, has to be taken when tuning these models and/or switching among PI models.

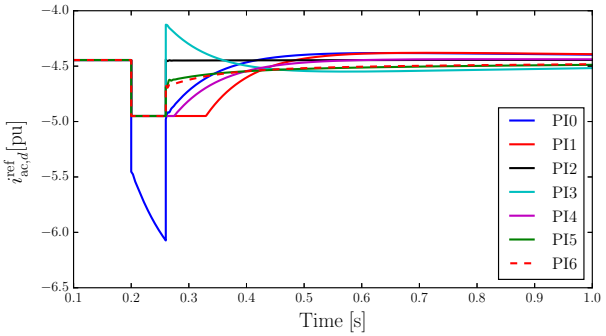

Fig. 7: Response of the output of the active power controller of the Irish-side VSC.

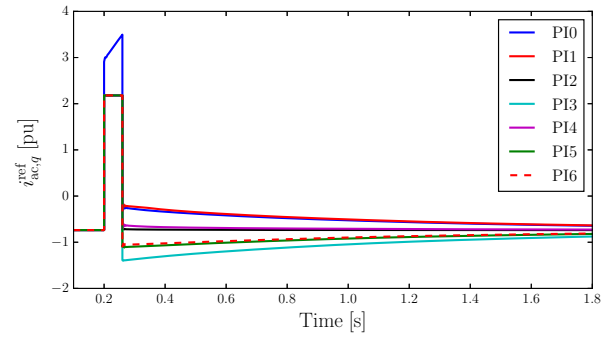

Fig. 8: Response of the output of the AC voltage controller of the Irish-side VSC.

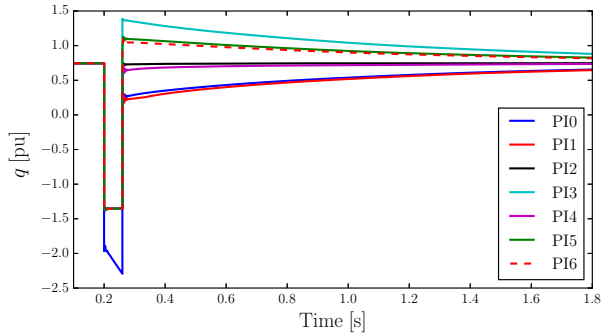

Fig. 9: Response of the reactive power support of the Irish-side VSC.

C. Case Study 2: STATCOM

The Nordic test system presented in [36] is used for this second case study. The system includes 74 buses; 102 branches, of which 20 step-up and 22 distribution transformers with under-load tap changers; 20 generators, of which 7 are round rotor and 13 are salient pole types, with TGs, AVRs, PSSs, and Over Excitation Limiters (OELs). Except for the OELs, which are models as in [19], all other models and data used in this case study match those reported in [36].

The STATCOM is a VSC-based shunt FACTS device utilized to regulate the voltage of the bus at which it is connected. A STATCOM is connected to the Nordic test system at bus 1044. STATCOM parameters and ratings are based on [37]. Except for some small losses, the STATCOM only exchanges reactive power with the grid. Thus the current limits of the VSC device are set in such a way that priority is given to the q-axis component. The d-axis current limit is set to a

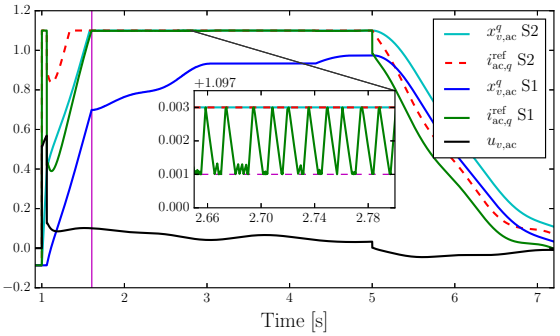

Fig. 10: Scenario (a): Response of the AC voltage controller of the outer level of the STATCOM, using models PI2-S1 and PI2-S2.

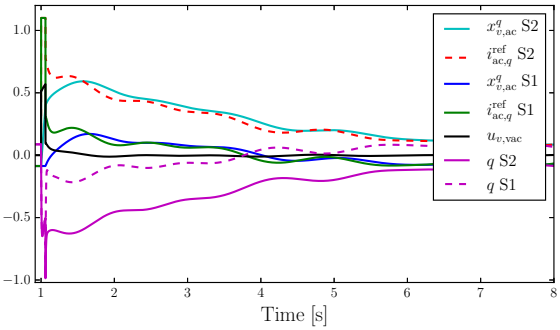

Fig. 11: Scenario (b): Response of the AC voltage controller of the outer level and reactive power support provided by the STATCOM, using models PI2-S1 and PI2-S2.

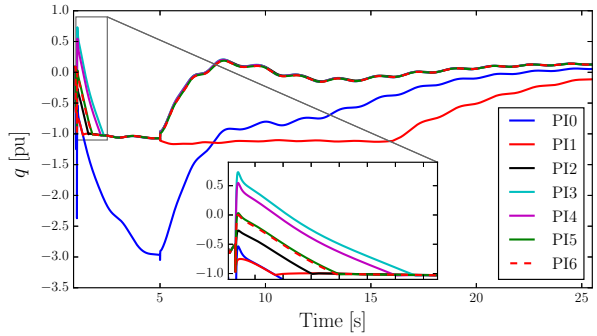

Fig. 12: Scenario (a): reactive power support from STATCOM, using models PI0 to PI6.

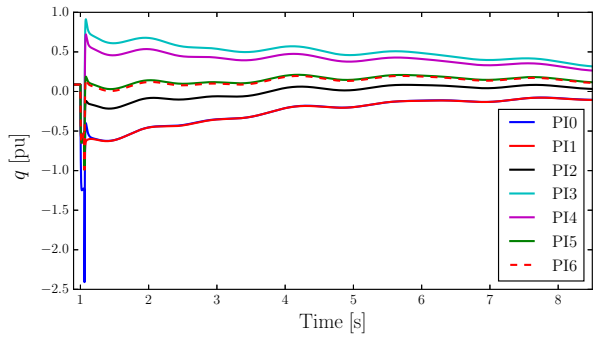

Fig. 13: Scenario (b): reactive power support from STATCOM, using models PI0 to PI6.

small value to allow regulating of the DC bus voltage and loss compensation.

1) Comparison of alternative solutions of IEEE standard: The comparison discussed in this section considers the dynamic response of the PI controllers following a three-phase fault at bus 4044, occurring at $t = 1$ s and cleared at $t = 1.06$ s. Two scenarios are studied: (a) the fault is cleared by opening the line between bus 4044-4032 at $t = 1.06$ s, then the line is re-closed at $t = 5$ s; and (b) the fault is cleared at $t = 1.06$ s without opening any line.

In both scenarios, the conventional implementation of model PI2 shows the numerical issues discussed in Section III-B. Using other integration methods, i.e., second order BDF and implicit backward Euler, and reducing the time step or changing to adaptive step size do not remove the deadlock problem. This allows comparing the performance of methods S1 and S2, discussed in Section III-B. The conventional PI2 model leads to a deadlock at $t = 1.605$ s (see the vertical line in Fig. 10). Model PI2-S1 with a DB of 0.002 allows completing the simulation. For model PI2-S2, which never shows the deadlock issue, the integrator is limited to the same values as the current reference limits.

Figures 10 and 11 show the trajectories of the q-axis current reference of the VSC outer control and its corresponding state ($x^q_{v,\mathrm{ac}}$) with the input ($u_{v,\mathrm{ac}} = v^{\mathrm{ref}}_{\mathrm{ac}} - v_{\mathrm{ac}}$) for both contingencies respectively. Figure 11 also shows the reactive power provided by the STATCOM.

While model PI2-S1 avoids the deadlock phenomenon, its transient response depends on the magnitude of the DB and the severity of the contingency. If the DB is too small or the contingency is too severe, the deadlock can occur again. Model PI2-S2 never shows the trajectory deadlock (at least according to our experience) but can lead to significant differences in the transient response and final steady-state conditions because the integrator state is not locked unless it hits a limit (see Fig. 11). Unfortunately, the exact values of such limits for integrator state are often unknown. Typically, same limits as the algebraic PI output are used, but this is not necessarily the best approach as the state variable can wind up independently (and inconsistently) with respect to the output of the PI.

2) Comparison of all PI models: Figures 12 and 13 show the reactive power response of models PI0 to PI6 using the scenarios (a) and (b) described in Section V-C1. DB=0.002 is used for model PI2-S1.

Compared to previous case study, the impact of PI model differences on the transient response is more significant. In particular, Fig. 12 shows that the response of models PI0 and PI1 are not acceptable. Back calculation models PI3 and PI4 leads the STATCOM to absorb reactive power whereas model PI2-S1 leads to the opposite behavior, at least for a few seconds. This mixed response can be changed by reducing the feedback gain value. However a high feedback gain value is recommended to reset the integrator quickly [1], [12]. Tracking methods with delay and the combined type (models PI5 and PI6) show better transient response than the other PI types considered in this case study.

D. Discussion on Simulation Results

PI models with AW limiters are to be preferred to windup ones due to their faster transient response. However, since there are several ways to implement AW limiters, it is difficult to anticipate the response of each PI model. Results depend not only on the PI model itself, but also on the severity of the disturbance, the PI parameters, network configuration and initial operating point.

For the IEEE PI model (PI2), a deadband (or hysteresis) or other numerical solutions can be required to avoid trajectory deadlock. This raises a variety of implementation issues. An early reference [38] suggests that this problem is not only a software issue due to the discretization of the integration scheme and that it can affect also the physical digital controller. However, in practice, the input quantities to the controller will eventually change and possibly unlock the device. On the other hand, in simulations, the deadlock prevents the integration scheme to converge and is thus critical to identify and/or avoid it with adequate software implementation "tricks." It is worth mentioning that PI2 is also tested in Modelica based software tool OpenModelica [39] where solvers are strictly separated from models. Solvers in OpenModelica also shows same numerical chattering issue as DOME shows.

Compared to the other AW types, model PI2 provides a better transient response, namely, fast convergence to post disturbance equilibrium, as well as low over- and under-shoot. It is also worth noticing that the deadlock issue does not occur if $k_p = 0$.

The main advantage of back calculation models PI3 to PI6 is that they intrinsically avoid the deadlock. There is also no difference in the response of the hardware and software implementations of these models. But they have other issues. Since the state variable of the integrator is never really locked, their time response is slower, which can deteriorate the overall performance of the VSC controllers. Then models PI3 to PI5 require tuning an extra parameter, and model PI6 is intrinsically complex due to the mix of continuous and discrete variables and logical operations. Tuning the back calculation gain or delay requires particular care because of their significant impact on the overall PI dynamic behavior.

Compared to [3], where only small networks are considered, the different implementations of PI controllers impact mostly the local behavior of the VSC devices. However, the test system considered in this paper are dominated by conventional synchronous generation and, hence, the dynamics of electronic converters have a smaller impact on the overall system than what observed in [3].

For high-dimensional nonlinear sets of differential-algebraic equations often the results can not be generalized. The best that can be done is to show possible issues and discuss why these issues appear. Based on the results of this paper, it is fair to conclude that the models of the limiters of the PI controllers can vary significantly the behavior of the VSC controllers, and, if the penetration of such devices is high, also that of the overall grid.

E. Remarks and Recommendations

1) Utilization and complexity of PI anti-windup limiter models: According to the literature, the most commonly used anti-windup method on a PI controller is the back calculation. Despite being a standard, the model described in the IEEE standard 421.5-2016 is less common and among all considered models, the IEEE standard, in fact, is the most complex as it requires to introduce a fictitious deadband to work properly. Models PI3 and PI4, on the other hand, are the simplest models.

2) Dynamic Performance: For small disturbances, e.g., load variations and line outages without faults, all PI models show very similar transient response, even if they saturate. This has to be expected as, for light disturbances, the differences in state variable between the PI models that lock their internal state variable (IEEE standard) and those that do not (back calculation, PI3-PI6) is small. So in this cases, models PI3 to PI6 are to be preferred as they do not create numerical issues.

On the other hand, significant differences of the dynamic response of the PI models are observed for large disturbances, e.g., faults and large generator outages. In these cases, the dynamic response of the IEEE standard PI model is the best choice as it locks the PI internal state variable and reduce the delay of the operation of the controller when the input signal is back to normal.

3) Best practice: For dynamic analysis of real-world power system networks the best practice is to carefully model PI controllers according to the actual hardware and specifications provided by the vendors of the VSC devices. If the real implementation is unknown, the choice becomes a trade-off between dynamic performance and implementation complexity. Whenever priority is the performance following a large disturbance, IEEE standard (PI2) is recommended. To avoid trajectory deadlock a deadband should be considered in the implementation. In order to avoid implementation complexity a back calculation method is preferred. In particular, we recommend the model PI4 and if a trial and error tuning technique is preferred to avoid complex tuning techniques, a convenient initial guess of the back calculation gain is $k_s \approx (1/t_i)$, where $t_i = \frac{k_p}{k_i}$, is the integral time constant [40].

VI. CONCLUSIONS

This paper reviews and compares the dynamic behavior of VSC-HVDC links and STATCOM device considering different PI controller models with windup and anti-windup limiters. Simulation results indicate that anti-windup limiters are to be preferred but their implementation and design require particular care. The PI model based on the IEEE Standard 421.5-2016 shows the fastest dynamic response but also the most critical implementation, which can lead to numerical issues.

Due to the world-wide trend to increase the penetration of VSC-based generation, it appears more and more important to pay attention to modelling aspects, such as PI limiters, that in the past have been often overlooked. The paper also distinguishes between modelling and solver issues to serve the

practitioners who deals with power system dynamic analysis and software implementation.

Future work will further investigate the inherent numerical issues of the implementations of the IEEE Standard 421.5-2016 and propose suitable solutions.

REFERENCES

[1] K. J. Åström and T. Hägglund, *Advanced PID Control*. ISA - The Instrumentation, Systems and Automation Society, 2006.

[2] A. H. Glattfelder and W. Schaufelberger, *Control systems with input and output constraints*. Springer Science & Business Media, 2012.

[3] M. A. A. Murad, Á. Ortega, and F. Milano, "Impact on power system dynamics of PI control limiters of VSC-based devices," in *Power Systems Computation Conference (PSCC)*, June 2018, pp. 1–7.

[4] A. Visioli, "Modified anti-windup scheme for PID controllers," *IEE Proceedings - Control Theory and Applications*, vol. 150, no. 1, pp. 49–54, Jan 2003.

[5] M. V. Kothare, P. J. Campo, M. Morari, and C. N. Nett, "A unified framework for the study of anti-windup designs," *Automatica*, vol. 30, no. 12, pp. 1869 – 1883, 1994.

[6] S. Tarbouriech and M. Turner, "Anti-windup design: an overview of some recent advances and open problems," *IET Control Theory Applications*, vol. 3, no. 1, pp. 1–19, January 2009.

[7] S. Galeani, S. Tarbouriech, M. Turner, and L. Zaccarian, "A tutorial on modern anti-windup design," *European Journal of Control*, vol. 15, no. 3-4, pp. 418–440, 2009.

[8] *IEEE recommended practice for excitation system models for power system stability studies*, IEEE Std 421.5-2016 (Revision of IEEE Std 421.5-2005), 26 Aug. 2016.

[9] M. Imhof and G. Andersson, "Dynamic modeling of a VSC-HVDC converter," in *Universities Power Engineering Conference (UPEC)*, Sept 2013, pp. 1–6.

[10] W. Qiao and R. G. Harley, "Power quality and dynamic performance improvement of wind farms using a STATCOM," in *IEEE Power Electronics Specialists Conference*, June 2007, pp. 1832–1838.

[11] J. Fang, W. Yao, Z. Chen, J. Wen, and S. Cheng, "Design of anti-windup compensator for energy storage-based damping controller to enhance power system stability," *IEEE Transactions on Power Systems*, vol. 29, no. 3, pp. 1175–1185, May 2014.

[12] I. A. Hiskens, "Trajectory deadlock in power system models," in *IEEE International Symposium of Circuits and Systems (ISCAS)*, May 2011, pp. 2721–2724.

[13] ——, "Dynamics of type-3 wind turbine generator models," *IEEE Transactions on Power Systems*, vol. 27, no. 1, pp. 465–474, Feb 2012.

[14] D. Fabozzi, S. Weigel, B. Weise, and F. Villella, "Semi-implicit formulation of proportional-integral controller block with non-windup limiter according to IEEE Standard 421.5-2016," in *Bulk Power Systems Dynamics and Control Symposium (IREP)*, 2017, pp. 1–7.

[15] F. Milano, "Semi-implicit formulation of differential-algebraic equations for transient stability analysis," *IEEE Transactions on Power Systems*, vol. 31, no. 6, pp. 4534–4543, Nov 2016.

[16] M. Tharayil and A. Alleyne, "A generalized PID error governing scheme for SMART/SBLI control," in *Proceedings of the 2002 American Control Conference*, vol. 1, May 2002, pp. 346–351 vol.1.

[17] "Simscape Power Systems," [Online]. Available: https://www.mathworks.com/products/simpower.html.

[18] J. Mahseredjian, S. Dennetière, L. Dubé, B. Khodabakhchian, and L. Gérin-Lajoie, "On a new approach for the simulation of transients in power systems," *Electric Power Systems Research*, vol. 77, no. 11, pp. 1514 – 1520, 2007.

[19] F. Milano, *Power system modelling and scripting*. Springer Science & Business Media, 2010.

[20] A. Ametani, *Numerical Analysis of Power system Transient Dynamics*. IET, London, 2015.

[21] F. Milano, "A Python-based software tool for power system analysis," in *IEEE PES General Meeting*, Vancouver, BC, 2013, pp. 1–5.

[22] D. Fabozzi, A. S. Chieh, P. Panciatici, and T. Van Cutsem, "On simplified handling of state events in time-domain simulation," *Proceedings of the 17th PSCC*, 2011.

[23] A. Bellen and M. Zennaro, *Numerical methods for delay differential equations*. Oxford: Oxford Science Publications, 2003.

[24] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1501–1508, July 2012.

[25] S. Chiniforoosh, J. Jatskevich, A. Yazdani, V. Sood, V. Dinavahi, J. A. Martinez, and A. Ramirez, "Definitions and applications of dynamic average models for analysis of power systems," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2655–2669, Oct 2010.

[26] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, *Multi-terminal direct-current grids: Modeling, analysis, and control*. John Wiley & Sons, 2014.

[27] Á. Ortega and F. Milano, "Generalized model of VSC-based energy storage systems for transient stability analysis," *IEEE Transactions on Power Systems*, vol. 31, no. 5, pp. 3369–3380, Sept 2016.

[28] J. Beerten, S. Cole, and R. Belmans, "Modeling of multi-terminal VSC HVDC systems with distributed DC voltage control," *IEEE Transactions on Power Systems*, vol. 29, no. 1, pp. 34–42, Jan 2014.

[29] H. Saad, J. Mahseredjian, S. Dennetière, and S. Nguefeu, "Interactions studies of HVDC-MMC link embedded in an AC grid," *Electric Power Systems Research*, vol. 138, pp. 202 – 209, 2016.

[30] A. A. van der Meer, M. Gibescu, M. A. M. M. van der Meijden, W. L. Kling, and J. A. Ferreira, "Advanced hybrid transient stability and EMT simulation for VSC-HVDC systems," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1057–1066, June 2015.

[31] L. R. da Silva, R. C. Flesch, and J. E. Normey-Rico, "Analysis of anti-windup techniques in PID control of processes with measurement noise," *IFAC-PapersOnLine*, vol. 51, no. 4, pp. 948 – 953, 2018.

[32] Y. Amirnaser and I. Reza, *Voltage-sourced converters in power systems: modeling, control, and applications*. IEEE Press, 2012.

[33] Á. Ortega and F. Milano, "Modeling, simulation, and comparison of control techniques for energy storage systems," *IEEE Transactions on Power Systems*, vol. 32, no. 3, pp. 2445–2454, May 2017.

[34] K. R. W. Bell and A. N. D. Tleis, "Test system requirements for modelling future power systems," in *IEEE PES General Meeting*, July 2010, pp. 1–8.

[35] J. Egan, P. O'Rourke, R. Sellick, P. Tomlinson, B. Johnson, and S. Svensson, "Overview of the 500 MW EirGrid East-West Interconnector, considering system design and execution-phase issues," in *Universities Power Engineering Conference (UPEC)*, Sept 2013, pp. 1–6.

[36] IEEE PSDP Committee Power System Stability Subcommittee Test Systems for Voltage Stability and Security Assessment Task Force, "Test systems for voltage stability analysis and security assessment," Technical Report PES-TR19, Tech. Rep., 2015.

[37] A. Oskoui, B. Mathew, J. P. Hasler, M. Oliveira, T. Larsson, A. Petersson, and E. John, "Holly STATCOM – FACTS to replace critical generation, operational experience," in *IEEE/PES Transmission and Distribution Conference and Exhibition*, May 2006, pp. 1393–1398.

[38] K. J. Åström and L. Rundqwist, "Integrator windup and how to avoid it," in *1989 American Control Conference*, June 1989, pp. 1693–1698.

[39] "OpenModelica," [Online]. Available: https://www.openmodelica.org/.

[40] K. J. Åström and R. M. Murray, *Feedback systems: an introduction for scientists and engineers*. Princeton university press, 2010.

Mohammed Ahsan Adib Murad (S'18) received B.Sc. degree in electrical engineering from Islamic University of Technology, Bangladesh in 2009, and double M.Sc. degree in Smart Electrical Networks and Systems from KU Leuven, Belgium and KTH, Sweden in 2015. He is currently pursuing the PhD degree with the department of electrical and electronic engineering, University College Dublin, Ireland. His current research interests include power system modelling and dynamic analysis.

Federico Milano (F'16) received from the Univ. of Genoa, Italy, the ME and Ph.D. in Electrical Eng. in 1999 and 2003, respectively. From 2001 to 2002 he was with the Univ. of Waterloo, Canada, as a Visiting Scholar. From 2003 to 2013, he was with the Univ. of Castilla-La Mancha, Spain. In 2013, he joined the Univ. College Dublin, Ireland, where he is currently Professor and Head of Electrical Engineering. His research interests include power system modelling, control and stability analysis.