Modeling and Simulation of Variable Limits on Conditional Anti-Windup PI Controllers for VSC-based Devices

Mohammed Ahsan Adib Murad, Muyang Liu, *Member, IEEE* and Federico Milano, *Fellow, IEEE*

***Abstract*—This work focuses on variable limits of conditional anti-windup PI-controller described in the IEEE Std. 421.5-2016 applied in the current limiters of VSC-based applications. To overcome deadlock and chattering during numerical simulation of the Std. conditional anti-windup with variable limits, it proposes a method for software implementation based on Filippov theory. The robustness of the proposed implementation is studied through a VSC-HVDC link included in the WSCC 9-bus system and through STATCOM included in the Nordic-32 system. The case studies compare wind up, back calculation type anti-windup and heuristic methods applied in the conditional anti-windup with the proposed solution.**

***Index Terms*—Proportional-integral control, anti-windup limiter, voltage-sourced converter, variable limit, current limitation.**

I. Introduction

A. Motivation

Different limiting methods on the Proportional and Integral (PI) controllers, for example, windup, anti-windup (AW) methods based on the back-calculation [1]–[4] or the conditional type defined by the IEEE Standard 421.5-2016 [5] are commonly employed on the PI controllers of Voltage-Sourced Converters (VSCs). Among the AW methods, the IEEE Std. AW method shows numerical issues (deadlock and chattering) during dynamic simulation [6]–[8]. To eliminate these issues a Filippov Theory (FT) based implementation with a constant limit on the Std. AW PI is proposed in [9]. However dynamic models of VSCs usually employ a variable limit on the PIs. However, references [6]–[9] do not tackle the numerical issues if the limits of the standard model are variable. This paper extends the FT based implementation proposed in [9] to impose variable limits. This paper also discusses the interaction between the current limiter of the VSCs and the PIs with various variable limiting implementations, which has not been studied thus far.

B. Literature Review

The integration of VSC-based resources into power systems is continuously increasing. The high-level controllers of VSCs include the most important control functions, e.g. active/reactive power control, AC/DC voltage control, Fault Ride-Through (FRT) functionality, current limitation. The response of these high-level controllers has a significant impact on power system dynamics [7], [10]. If these controllers of the VSCs are PI and are coupled with a current limiter, several configurations are possible, including constant limits (see [I] in Fig. 3); virtual impedance-based current limiter; and variable limits with either wind-up or anti-windup variable limits (see [II] and [III] in Fig. 3). Constant current limits are utilized in most papers, e.g. [1], while the virtual impedance approach is used in [11]. In this paper, we study grid-following VSC converter models with variable current limits.

The working principle of the current limiting of VSCs depends on the priority of a quantity of interest. The choice of this priority depends on the VSC applications, for example: HVDC [12], FACTS [13], Type-3 and Type-4 Wind-Generator [14], [15] and Energy Storage [16]. For instance, if the converter is connected to a heavily loaded area with possible voltage issues, the priority is given to the reactive power. This ensures reactive power support when the current limit is exceeded, and the remaining current is available for active power production. Transient stability assessment of power systems considering discontinuities of current limiters are performed based on numerical time domain simulation due to the lack of available analytical methods e.g., Lyapunov function [17]. Therefore during numerical simulation it is important take account time varying limits on the PI controllers of VSCs. However if the IEEE Std. AW model is used with varying limits it suffers similar numerical issues e.g., deadlock and chattering as discussed in [9]. Until now a deadlock and chattering free IEEE Std. AW PI controller model with variable limits is not available in the literature. The focus of the paper is on the numerical issues of variable limits on conditional anti-windup PI-controller described in the IEEE Std. 421.5-2016, applied in the current limiters of VSC-based applications.

To overcome the numerical issues with the Std. AW PI model with constant limits, previous studies proposed several solutions. In [6], [18] a deadband based technique is discussed, however this technique does not remove artificial chattering. In [19] a semi-implicit modeling approach is proposed. This semi-implicit model does not propose any solution if the limits are variable. We proposed a model in [9] based on the mathematical theory developed by Filippov applicable to dynamical systems with discontinuous right hand side [20]. Our previous study [9] considered only constant limits. The

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This work was supported by Science Foundation Ireland (SFI) under Grant No. SFI/15/IA/3074.

switching conditions derived in [9] to move from one discrete state to another (e.g., integration state to maximum) of the IEEE Std PI controller during time domain simulation are not adequate if the limits of become variable. Therefore, this paper extends and validates the FT based Std. AW model to impose variable limits; studies impact of time-varying limits on dynamic performance of VSC-based devices. Moreover, a modified deadband based IEEE Std. AW is also proposed to remove the chattering on the controller outputs.

C. Contributions

The specific contributions of the paper are as follows.

- A Filippov theory based IEEE Std. conditional AW PI model for implementation in power system tools for dynamic analysis to consider variable limits in VSC-based applications.
- A modification of the deadband based implementation of the Std. AW model to remove chattering on the output.
- The impact of current limitation of VSCs coupled with different PI implementations on the dynamic response.

It is relevant to note that some commercial software packages have their own solutions to overcome the numerical challenges that are discussed in this paper. However, to the best of our knowledge, such solutions are mostly heuristic and, more importantly, are not published and made available in the literature. The value of our work is thus twofold: (i) it tackles a numerical problem that is relevant to industry as it affects the models of widely used power system devices and controllers; and (ii) it provides a general and systematic mathematical framework for the solution of such a problem that can be reproduced by researchers and practitioners in any computer language, e.g., Modelica or Python.

D. Organization

The remainder of the paper is organized as follows. Section II presents the VSC model, its control, current limitation and fault ride-through functionalities. Section III discusses the IEEE Std. AW PI model with variable limits and extends the FT and DB based designs to impose variable limits. Section III also validates the both models through an illustrative example. Section IV illustrates the dynamic behavior of VSCs through two case studies: (i) a VSC-HVDC link in the WSCC 9-bus network; (ii) the Nordic system with a VSC-based STATCOM. Finally, Section V draws conclusions.

II. Voltage-Sourced Converter

The model of the converter of the VSC is an average value model which includes a transformer in the AC side, a bi-directional AC/DC converter, a condenser, a pulse-width modulation and a two-level control (see Fig. 1). The interested reader can find the complete formulation of the converter model in [1]. In the remainder of this section we focus exclusively on the models of the controllers.

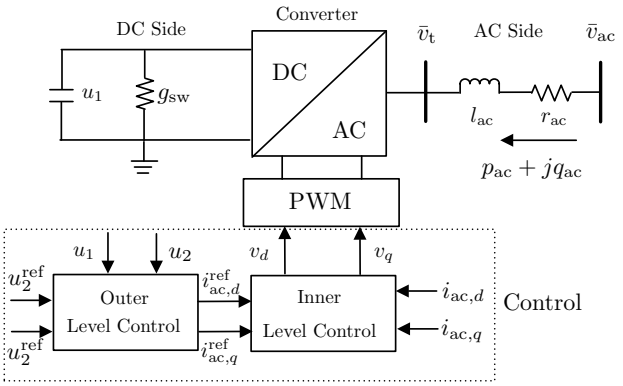

Fig. 1: VSC converter with its inner and outer control in dq-frame.

A. Converter Control

Figure 2 shows the vector-current control considered in this paper. This control strategy uses a dq-composition with the grid voltage as phase reference, an inner current control loop to decouple the current into its d- and q-components. The reference currents for the inner control are achieved using an outer or high level controller loop.

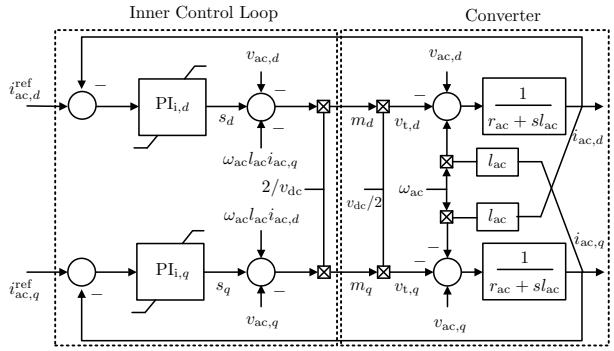

Fig. 2: VSC converter and inner current control in dq-frame.

An outer control loop utilizes the d-component to control active power or DC voltage, and the q-component to control reactive power or AC voltage. Both inner and outer loops are implemented with PI controllers. Based on the current limiting method of the VSCs, the outer control loop can have a constant or variable limits. Figure 3 shows three possible configurations for the outer control loop. Configuration [I] is a conventional model with constant limit. The other two configurations, i.e. [II] and [III], are most relevant for this paper as they define wind-up and anti-windup, respectively, variable limiters.

B. Current Limitation

The configurations [II] and [III] in Fig. 3 include a "current limit logic" block that limits the converter current references in the upper-level control of the VSCs. The outputs of the current limit logic determine the limits of the d- and q-axis of the PI controllers (see Fig. 3) used in the outer level of VSCs. FRT capabilities are also coupled into this block. This section discusses the working principle of the current limit logic.

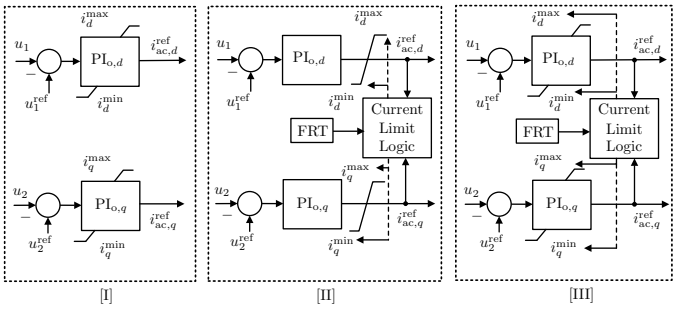

Fig. 3: Outer control configurations: [I] constant limits; [II] variable limits with wind-up PIs and [III] variable limits with AW PIs.

1) Active Power or DC voltage Priority: If the priority is given to the active power or DC voltage, $i^{\text{ref}}_{\text{ac},d}$ is limited to the d-axis current limit whereas $i^{\text{ref}}_{\text{ac},q}$ is limited in such a way that the total current does not exceed the maximum current rating of the converters, as follows:

$$\begin{aligned} i_d^{\max} &= i_d^{\text{lm}} \ , \\ i_d^{\min} &= -i_{\text{ac},d}^{\max} \ , \\ i_q^{\max} &= \min(\sqrt{i_{\max}^2 - i_{\text{ac},d}^2}, i_q^{\text{lm}}) \ , \\ i_q^{\min} &= -i_{\text{ac},q}^{\max} \ , \end{aligned} \tag{1}$$

where, $i_{\max}$, i_d^{lm} and i_q^{lm} are the maximum current capacity of the converter, d-axis current limit and q-axis current limit respectively; $i_d^{\max}$, $i_d^{\min}$, $i_q^{\max}$ and $i_q^{\min}$ are the time varying limits of the PIs in the outer level control (see Fig. 3). Note that, i_d^{lm} and i_q^{lm} can be set as equal or less than $i_{\max}$ [21].

2) Reactive Power or AC voltage Priority: If the priority is given to the reactive power or AC voltage, $i^{\text{ref}}_{\text{ac},q}$ is limited by the q-axis current limit whereas $i^{\text{ref}}_{\text{ac},d}$ is limited in such a way that the total current does not exceed the maximum current rating of the converters, as follows:

$$\begin{aligned} i_q^{\max} &= i_q^{\text{lm}} \ , \\ i_q^{\min} &= -i_{\text{ac},q}^{\max} \ , \\ i_d^{\max} &= \min(\sqrt{i_{\max}^2 - i_{\text{ac},q}^2}, i_d^{\text{lm}}) \ , \\ i_d^{\min} &= -i_{\text{ac},d}^{\max} \ . \end{aligned} \tag{2}$$

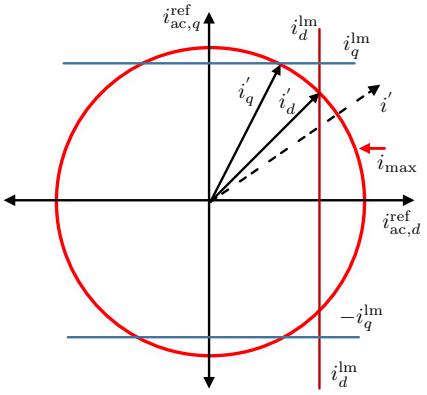

Fig. 4: Geometrical representation of the current limit logic.

A graphical representation of the current limit logic is shown in Fig. 4. In this figure, i_d' and i_q' are the currents with active and reactive power priority respectively; i' is the total current without any bound.

3) Fault Ride Through: To comply with grid codes, VSC-based applications consider an FRT specification. Usually, FRT is activated if the AC voltage deviates from a pre-defined deadband/bound subjected to a disturbance. When FRT is activated, the controller switches its priority to reactive power for ac voltage support [22]. Moreover, during FRT, the q-axis controller can be replaced with a proportional control [21]. The FRT specification can define the gain of the proportional controller. In this paper, if the AC voltage at the bus where the VSC is connected falls below 0.9 pu the FRT is activated, and priority is switched to reactive power support. Only if the voltage level returns within 0.92 pu, the current limit logic switches off the FRT.

III. Variable Limits on Anti-Windup PI

Among different AW methods, the IEEE Std. conditional AW is the preferred one for power system transient stability studies. This section first presents this model and extends the FT-based design in [9] to consider variable limits. The proposed novel DB-based implementation is also discussed in this section.

A. Conditional Anti-Windup PI Control

The conditional integration AW method defined by the IEEE Std. 421.5-2016 is as follows [5],

$$\begin{aligned} &\text{If } y \geqslant w^{\max} : w = w^{\max} \text{ and } \dot{x} = 0 \ , \\ &\text{If } y \leqslant w^{\min} : w = w^{\min} \text{ and } \dot{x} = 0 \ , \\ &\text{Otherwise} : w = y = k_p u + x \text{ and } \dot{x} = k_i u \ , \end{aligned} \tag{3}$$

where u, y, x, k_p, k_i, w, $w^{\max}$ and $w^{\min}$ are the input, output without limits, state variable, proportional and integral gains, limited output of the controller, maximum and minimum limits, respectively.

1) Filippov Theory-based Implementation: Filippov theory describes the necessary conditions for trajectory continuation of discontinuous right-hand side first-order ordinary differential equations [20]. This theory has been applied to study sliding bifurcations e.g., [23], [24] . This theory is outlined in Appendix A.

In this work, power system models are formulated as Hybrid Differential Algebraic Equations (HDAEs) as follows.

$$\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}, \boldsymbol{y}, \boldsymbol{z}) \ , \tag{4}$$

$$\boldsymbol{0} = \boldsymbol{g}(\boldsymbol{x}, \boldsymbol{y}, \boldsymbol{z}) \ , \tag{5}$$

where $\boldsymbol{x}$, $\boldsymbol{y}$ and $\boldsymbol{z}$ are the vector of state, algebraic and discrete variables respectively. Therefore the input to a PI controller can be an algebraic or a state variable depending on the application. However, FT is based exclusively on ODEs. References [25]–[27] describe two methods that allow applying FT to HDAEs. These methods are briefly discussed below.

- The first method converts the HDAEs into ODEs. For example, if (5) can be re-write as $\boldsymbol{y} = \boldsymbol{k}(\boldsymbol{x}, \boldsymbol{z})$, then (4) can be converted into $\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}, \boldsymbol{k}(\boldsymbol{x}), \boldsymbol{z})$. However, in power system models, the relation in (5) is non-linear and it is not trivial to convert the HDAEs into ODEs.
- The second method considers directly the HDAEs described by (4) and (5). However due to the lack of a theory on the coupling between the algebraic equations during sliding this method is still an open research topic [28].

Considering the limitations of the available methods to apply FT directly into all form of HDAEs, this section presents a FT-based modular and general-purpose model of the IEEE Std. AW PI controller that is compatible with HDAEs.

Let us consider the PI controller in Fig. 5. The derivation of necessary switching conditions according to Filippov theory to move from one discrete state to another (e.g., integration state to maximum state) without any numerical issues requires the approximation of the changes in the input and limits. Therefore, two low pass filters with time constants T and T_1 (see Fig. 5) are considered. This system is represented by (3) and

$$\begin{aligned} \dot{u} &= (v_1 - u)/T \ , \\ v_1 &= v - v^{\text{ref}} \ , \\ \dot{w}_{\max} &= (u_1 - w_{\max})/T_1 \ , \end{aligned} \tag{6}$$

where v_1 is the controlled signal, v^{ref} is the reference signal, u_1 is time varying input signal.

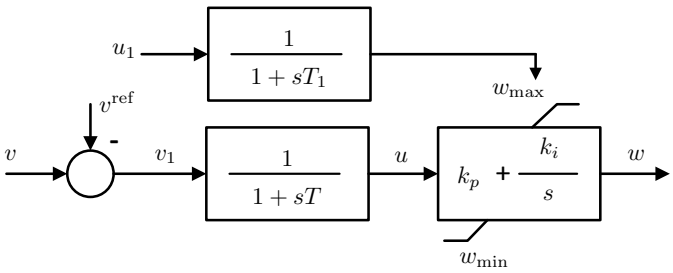

Fig. 5: IEEE Std. 421.5-2016 anti-windup PI controller with variable limits.

To apply FT, the state-space model considering the upper limit is as follows:

$$\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}) = \begin{cases} \boldsymbol{f_1}(\boldsymbol{x}) & \text{if } h(\boldsymbol{x}) < 0 \ , \\ \boldsymbol{f_2}(\boldsymbol{x}) & \text{if } h(\boldsymbol{x}) > 0 \ , \end{cases}$$

with

$$\boldsymbol{f_1}(x) = \begin{pmatrix} (v_1 - u)/T \\ k_i u \\ (u_1 - w_{\max})/T_1 \end{pmatrix}, \ \boldsymbol{f_2}(\boldsymbol{x}) = \begin{pmatrix} (v_1 - u)/T \\ 0 \\ (u_1 - w_{\max})/T_1 \end{pmatrix},$$

and the switching surface Σ is defined by zero of $h(\boldsymbol{x}) = y - w_{\max} = k_p u + x - w_{\max}$ and

$$h_x^T(\boldsymbol{x}) = [\frac{\partial h(x)}{\partial u} \quad \frac{\partial h(x)}{\partial x} \quad \frac{\partial h(x)}{\partial w_{\max}}] = [k_p \quad 1 \quad -1] \, .$$

Hence:

$$\begin{aligned} r_1(x) &= (k_p \quad 1 \quad -1) \begin{pmatrix} (v_1 - u)/T \\ k_i u \\ (u_1 - w_{\max})/T_1 \end{pmatrix} \\ &= k_p\big((v_1 - u)/T\big) + k_i u - (u_1 - w_{\max})/T_1 \ , \\ r_2(x) &= (k_p \quad 1 \quad -1) \begin{pmatrix} (v_1 - u)/T \\ 0 \\ (u_1 - w_{\max})/T_1 \end{pmatrix} \\ &= k_p\big((v_1 - u)/T\big) - (u_1 - w_{\max})/T_1 \ . \end{aligned} \tag{7}$$

The sliding vector filed becomes:

$$\begin{aligned} \alpha(x) &= \frac{k_p((v_1 - u)/T) + k_i u - (u_1 - w_{\max})/T_1}{k_i u} \ , \\ \boldsymbol{f_F}(\boldsymbol{x}) &= \begin{pmatrix} (v_1 - u)/T \\ -k_p((v_1 - u)/T) + (u_1 - w_{\max})/T_1 \end{pmatrix} \ . \end{aligned} \tag{8}$$

Therefore, for a software-based implementation of the FT-based AW PI model with variable limits the integrator differential equations, as follows:

$$\dot{x} = k_i u \, z_1 + \big(-k_p(v_1 - u)/T + (u_1 - w_{\max})/T_1 \big) \, z_2 \ ,$$

where z_1 and z_2 are discrete variables. Depending on the values of z_1 and z_2, e.g., 1 or 0 the right hand side of integrator state variable is switched to consider proper vector field. The state transition diagram for software implementation is given in Fig. 6, where the state INT and MAX represent integration and maximum state of the PI controller. The conditions to move from one state to another are evaluated when the switching function crosses zero. During sliding the exit conditions are calculated based on (15) i.e., based on $\alpha = 0$ and $\alpha = 1$. The lower limit can be implemented following a similar procedure.

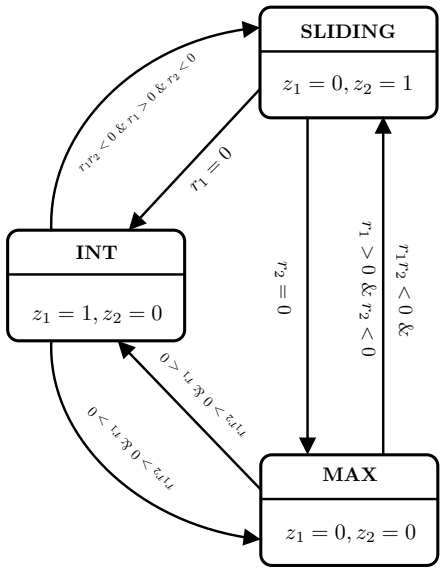

Fig. 6: State transitions of the IEEE Std. anti-windup PI controller with variable limits based on Filippov theory.

It is relevant to observe that to derive accurate switching conditions and the sliding vector field we introduced two time constants T, T_1. These should be tuned so that its dynamic

is faster than that of the PI controller. If in a power system application the input and limits are algebraic variable, one can implement this AW PI model without considering these two parameters. Because during numerical simulation it is possible to know the value of an variable from previous time step. For example, observe that during sliding (8), the right-hand side of the integrator state variable is the sum of decrease in the proportional channel and increase in the variable limit. However, the main advantage of this FT-based design is the ability to provide accurate switching conditions to remove numerical issues for implementation in any power system tool.

2) Deadband-based Implementation: The state transition diagram of the deadband-based implementation presented in [18] is the same when the limits are variable. As opposed to the implementation in [18], a modification of the conditions to switch the right-hand side of the time derivative of the integrator state variable is proposed. This modification removes the chattering on the bounded variable (w) during a deadlock situation. This feature is illustrated through the case studies presented in the next section.

The state transitions of the previous and the modified methods are shown in Fig. 7, where superscripts ^{a} is the method proposed in [18] (DB1) and ^{b} shows our modified method (DB2). For this kind of deadband techniques (DB1 and DB2), we show the state transitions to provide a mathematical formulation for software implementation. Thus, following the Fig. 7 a modeler can choose different implementation strategies for example, Hybrid Automata (HA) [29] or differential-algebraic impulsive switched [18] structure. In this work, we consider HA for the implementation of DB1 and DB2.

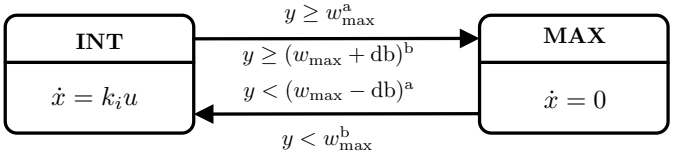

Fig. 7: State transitions of the anti-windup PI controller for existing solutions: superscripts a and b indicate the deadband-based techniques DB1 and DB2, respectively.

B. Illustrative Example

The two PI controllers shown in Fig. 3 (configuration [III]) with arbitrary inputs are considered as an illustrative example to validate the DB- and FT-based implementations of the IEEE Std. PI model. The current limiter controls the limits of both PI controllers. The priority is given to the d-axis current. The parameters are given in Table I.

TABLE I
Parameters of the illustrative example

Name	Values
PI_d	$k_p = 1$, $k_i = 10$
PI_q	$k_p = 1$, $k_i = 30$
Cur. Limiter	$i_{\max} = 1.02$, $i_d^{\mathrm{lm}} = 1.02$

This example is implemented in DOME [30] and Modelica [31] based tool Dymola [32]. In both sofware tools, the simulation is carried out using both the DB-based (DB1 and DB2) and FT-based implementations. The time-varying inputs to the PI controllers (PI_d and PI_q) are shown in Fig. 8.

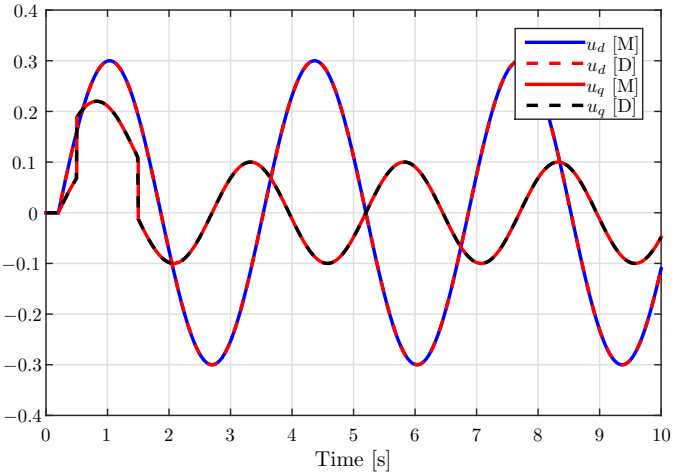

Fig. 8: Inputs to the PI_d and PI_q in Modelica ([M]) and DOME ([D]).

The output of PI_d hits the limit several occasions for the inputs (see Fig. 8) and as the priority is given to this controller, the maximum and minimum values of this controller do not change during the simulation. However, the limit values of PI_q are updated following the current limit logic (1) during the simulation. For all these three implementations, only the DB1-based method shows chattering in the limit values. This is because of the chattering of the output of the PI_d controller during a deadlock region.

The response of the outputs of the PI_d and PI_q are shown in Fig. 9. The outputs do not exceed the maximum limit (see Table I) and follow the current limit logic. Moreover, they show similar responses, and only the DB1-based method shows chattering on the output. DB2 and Filippov methods do not show chattering on the output. However, the DB2 method shows chattering on the state variable. This is illustrated in Figs. 10-11. Therefore, the Filippov based model overcomes possible numerical issues and provides an accurate dynamic response.

IV. Case Study

This section illustrates the impact of three different PI controller configurations utilized in VSC-based devices with current limit logic on the dynamic response of power systems. The three PI controller configurations are: windup (PI1), anti-windup with back calculation (PI3) and the IEEE Std. PI model (PI2). For the Std. model, the deadband-based methods (DB1 and DB2) and the FT-based solution methods are considered. Two applications of VSC-based devices are discussed: (i) a point-to-point VSC-HVDC link (Section IV-A); and (ii) a STATCOM device (Section IV-B). The case study of VSC-HVDC link considers the WSCC 9-bus system, whereas the case study on the STATCOM considers the Nordic-32 system. The power system software tool DOME [30] is utilized to carry out all simulations.

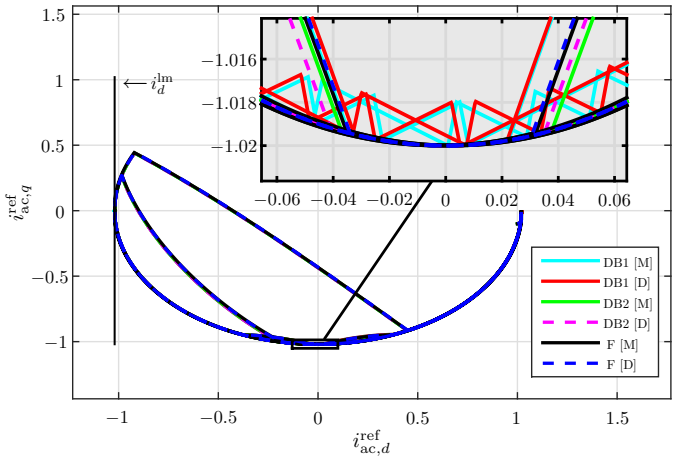

Fig. 9: Response of the outputs of the PI_d and PI_q controllers in DOME ([D]) and Modelica ([M]).

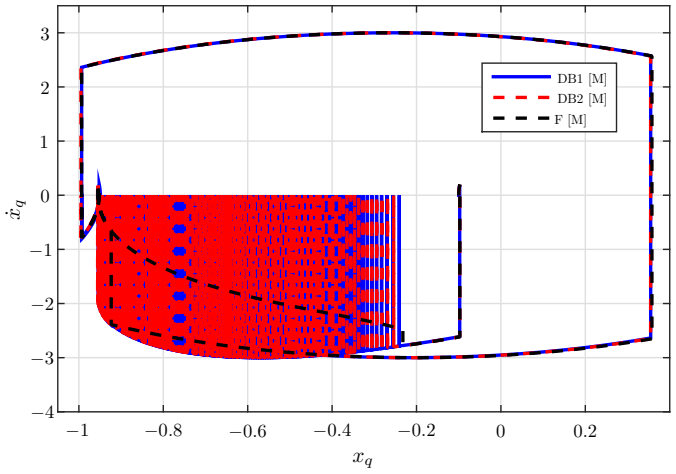

Fig. 10: Time derivative of the integrator state variable with the state variable of the PI_q controller in Modelica ([M]) using DB1, DB2 and Filippov based implementation.

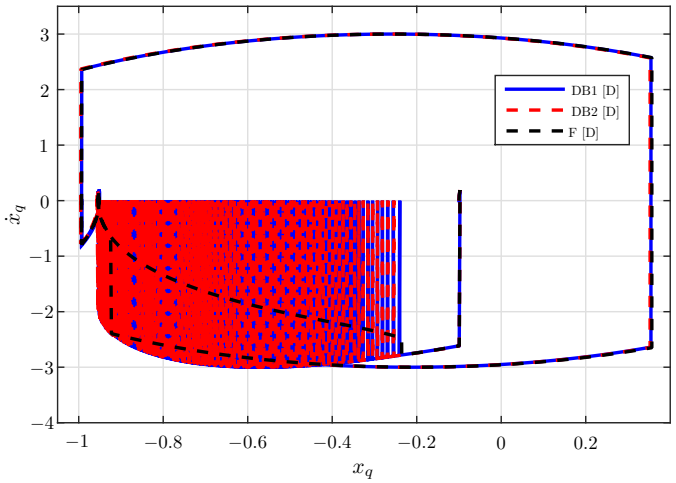

Fig. 11: Time derivative of the integrator state variable with the state variable of the PI_q controller in DOME ([D]) using DB1, DB2 and Filippov based implementation.

A. Case Study 1: VSC-HVDC Link

This case study is based on the WSCC 9-bus system described in [33]. The test network consists of three Synchronous Generators (SGs), three two-winding transformers, three loads and six transmission lines. All generators are equipped with Automatic Voltage Regulators (AVRs) and Turbine Governors (TGs). The transmission line that connects buses 7 and 8 is replaced with a VSC-HVDC Link. The original operating condition is assumed, i.e. 76 MW active power is transferred through the HVDC lines. The converter at bus 7 (VSC1) is acting as an inverter (converts AC to DC) and the one at bus 8 (VSC2) is acting as a rectifier (converts DC to AC).

VSC1 controls the DC voltage and AC voltage of bus 7 and VSC2 controls the active power and AC voltage of bus 8. The priority for the current limiters of VSC1 and VSC2 is DC voltage and active power, respectively, i.e. d-axis current. FRT is included in both VSCs. Two scenarios are studied with different current limit values, as shown in Table II. For both scenarios, the contingency is a three-phase fault at bus 5 that occurs at 0.1 s and cleared after 150 ms by opening the line that connects the buses 4 and 5. The magnitude of the deadband is 0.001 for the deadband-based PI implementations in the VSCs.

TABLE II
Parameters of current limit logic of VSCs

Parameters	Scenario I		Scenario II	
	VSC1	VSC2	VSC1	VSC2
Priority	v_{dc}	p	v_{dc}	p
i_d^{lm}	1.1 pu	1.1 pu	1.1 pu	1.1 pu
i_q^{lm}	1.1 pu	1.1 pu	0.5 pu	0.5 pu
$i_{\max}$	1.1 pu	1.1 pu	1.1 pu	1.1 pu

1) Scenario I: Figure 12 shows the voltage response at bus 7 following the contingency. In this scenario, the Std. PI model does not show any deadlock or chattering issues. The implementations based on the deadband and the Filippov approach show a similar transient response. For this reason only results for the Std. model with DB1-based implementation are shown. Anti-windup models show a very similar dynamic response. However, the PI1 shows a significantly different transient response with numerous chattering. To further illustrate the chattering, Fig. 13 shows the variation of the maximum limits and reference current outputs of $\text{PI}_{\text{o},d}$ and $\text{PI}_{\text{o},q}$ of the outer level of VSC1.

Immediately after the fault occurs, the bus voltage falls under 0.9 pu and the FRT is activated. This causes the priority to switch to reactive power or q-axis current. As the d-axis current limit (i_d^{lm}) and the q-axis current limit (i_q^{lm}) are equal to the maximum current capacity ($i_{\max}$) after the switching of priority the maximum limit of the $\text{PI}_{\text{o},d}$ falls to zero (see Fig. 13). The current reference follows this variable limit. At the same time, the limiter of the $\text{PI}_{\text{o},q}$ reaches the maximum current, as shown in Fig. 13. This enables maximum reactive power support from the VSC1. Note that while all PI controllers are at their limits, the state variables of PI1, PI2 and PI3 show different behaviors. Using PI1, after clearing

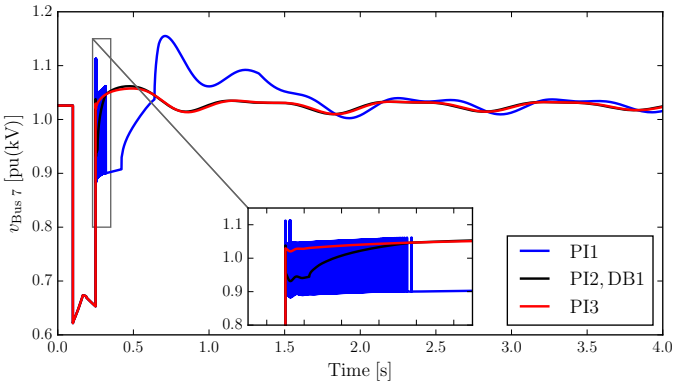

Fig. 12: Scenario I: Response of the bus voltage ($v_{\text{Bus }7}$) considering PI1, PI2 (DB1) and PI3.

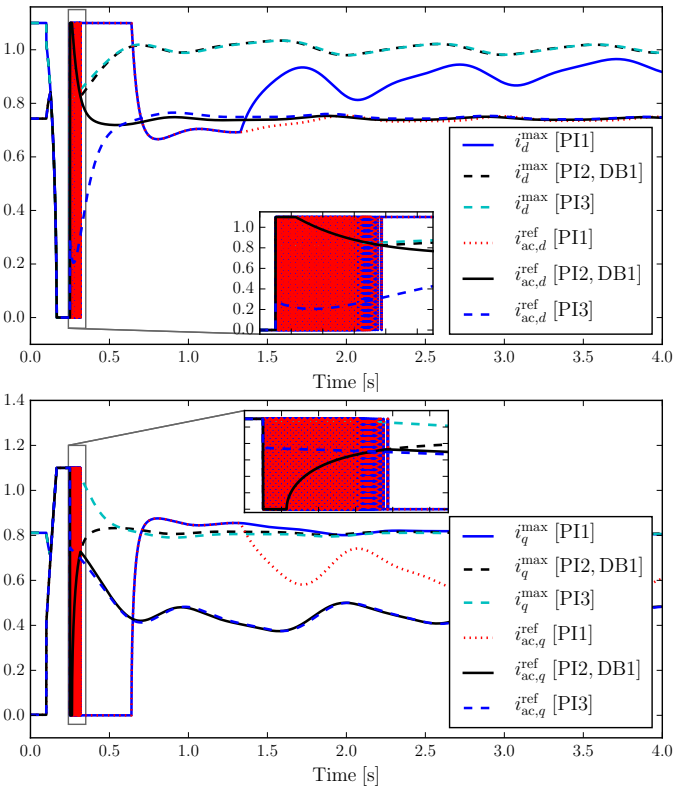

Fig. 13: Scenario I: Response of the maximum limit and the output current reference of $\text{PI}_{\text{o},d}$ (up) and $\text{PI}_{\text{o},q}$ (below) considering PI1, PI2 (DB1) and PI3 in VSC1.

the fault once the bus voltage returns in the safe operating margin (> 0.92 pu) the priority switches back to the d-axis current. Due to the windup effect, the d-axis reference current moves to the maximum current. This immediately results in the zero current reference for the q-axis controller and the reactive power support is ceased. This, in turn, lowers the voltage from 0.9 pu and the priority again switches backs to the q-axis current. The switching of priorities continues for a while and leads to chattering (see the zoomed detail in Fig. 13). Chattering significantly impacts on the performance of the numerical simulation and can give raise to deadlocks.

2) Scenario II: In this scenario, the i_q^{lm} is lower than the maximum current capacity in both VSCs. Following the contingency the reference currents of $\text{PI}_{\text{o},d}$ and $\text{PI}_{\text{o},q}$ in VSC1 are shown in Figs. 14-15 respectively for all the considered PI models. These figures also include DB1, DB2 and FT-based models for PI2. After the contingency, the priority is switched to the reactive power and the q-axis current reference reaches its limit (see Fig. 15). While it stays at its limit, the rest of the current is available for d-axis current reference and this is why this current reference does not reach to zero. Comparing with Scenario I and II, it is evident that the the current limit logic and the choice of the priority plays a significant role in the dynamic response during a severe disturbance.

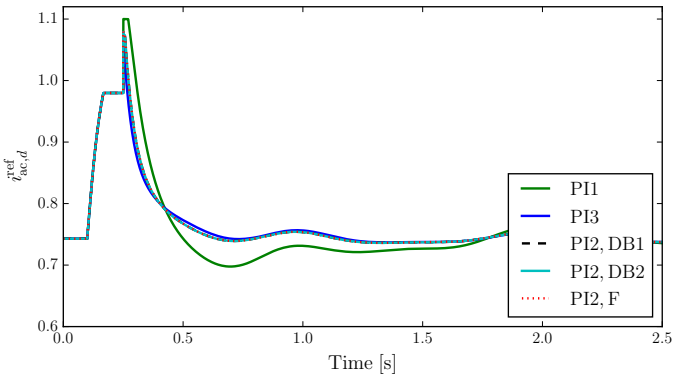

Fig. 14: Scenario II: Response of the output current reference of $\text{PI}_{\text{o},d}$ considering PI1, PI2 (DB1, DB2 and F) and PI3 in VSC1.

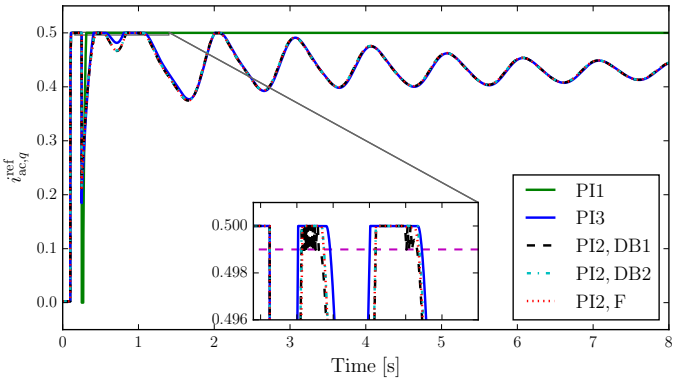

Fig. 15: Scenario II: Response of maximum limit and output current reference of $\text{PI}_{\text{o},q}$ considering PI1, PI2 (DB1, DB2 and F) and PI3.

The PI2 model gives raise to numerical chattering. Comparing DB1, DB2 and FT-based techniques, only DB1 based method results in chattering both in the output and the state variable (see zoomed details in Fig. 15 and Fig. 16). And the DB2 method does not show chattering on the output. Finally, Fig. 16 illustrates the time derivative of the state variables of PI2 and PI3 with respect to their state variable, and FT-based approach does not give raise to chattering in state variables.

B. Case Study 2: STATCOM

This Section considers the Nordic system presented in [34] with a VSC-based STATCOM. The system includes 74

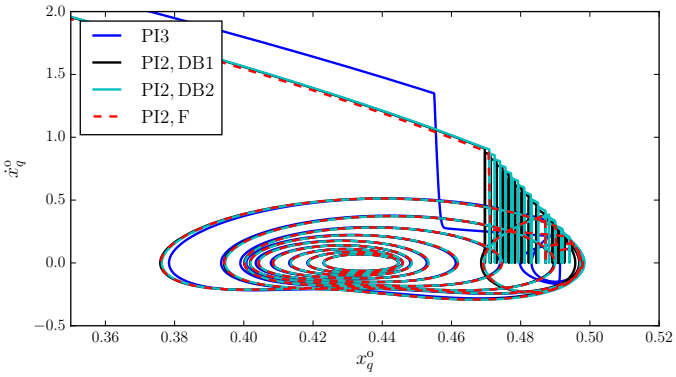

Fig. 16: Scenario II: time derivative of the integrator state variable with respect to the state variable of $\text{PI}_{o,q}$ in VSC1, considering PI3 and PI2 with DB1, DB2 and Filippov method.

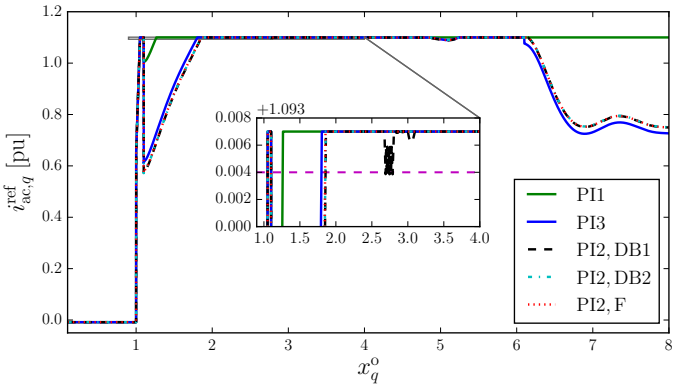

Fig. 17: Scenario I: Response of the AC voltage controller.

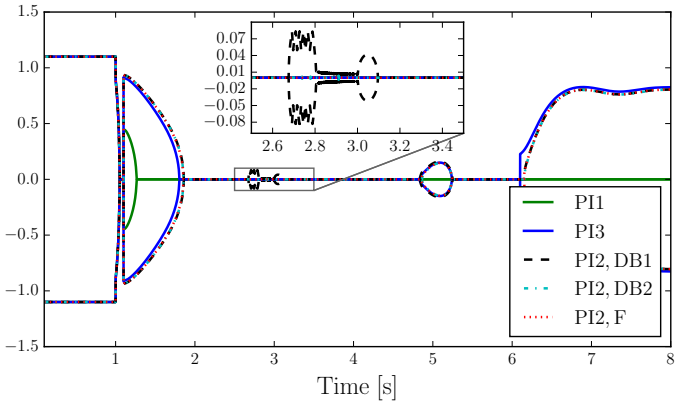

Fig. 18: Scenario I: Response of the $\pm\sqrt{i_{\max}^2 - i_{ac,q}^2}$.

buses; 102 branches, of which 20 step-up and 22 distribution transformers with Under Load Tap Changers, 20 generators, of which 7 are round rotor and 13 are salient pole types, with Turbine Governors, AVRs, PSSs, and Over Excitation Limiters. The system consists of four areas: North, Central, Equivalent and South. The base case of the system is heavily loaded with large power transfers from North to Central areas.

The d- and q-axis controllers of the outer level are set to control DC and AC voltage respectively. The STATCOM provides reactive power support, so the priority is set to q-axis current. Therefore, no switching of priority is needed. The contingency is a three-phase fault at bus 4044 occurring at $t = 1$ s and cleared by opening the line between bus 4044-4032 after 100 ms. The line is put back in service at $t = 6.1$ s. A deadband value 0.003 is used for DB1 and DB2 based PIs. Similar to the previous case study, two scenarios are studied and parameters of current limit logic are given in Table III. Both scenarios are discussed below.

TABLE III
Parameters of current limit logic of the STATCOM

Parameters	Scenario I	Scenario II
Priority	v_{ac}	v_{ac}
i_d^{lm}	0.05	0.05
i_q^{lm}	1.1	1.099
i_{max}	1.1	1.1

1) Scenario I: The trajectories of the q-axis current reference, $\pm\sqrt{i_{\max}^2 - i_{ac,q}^2}$ of the d-axis controller ($\text{PI}_{o,d}$), i.e. the DC voltage controller and the DC voltage are shown in Figs. 17, 18 and 19 respectively for the considered PIs. Following the contingency, the q-axis current reference reaches its maximum limit and the current limiter imposes zero on the limits of the d-axis controller (see Fig. 18). Using the PI2 model, the q-axis current reference limit stays longer at its limit due to windup and during this time, the d-axis current reference is zero. It causes an increasing trend in the DC voltage response. Such a deviation of the v_{dc} from its pre-disturbance equilibrium results in the collapse of the system.

For the AW methods, while $i_{ac,q}^{ref}$ stays at its limit, the PI2 model with DB1 and DB2 shows chattering, the PI3 and PI2 model with Filippov method show a smooth response. However, in this system chattering on the output ($i_{ac,q}^{ref}$) for the PI2 with DB1 causes a significant difference on the limits (see zoom in Fig. 18) of the d-axis controller compared to the other AW PIs. That is why a notable difference in the v_{dc} is observed with DB1. Scenario I shows that the same AW method depending on the implementations, can have a remarkable impact on the dynamic response. Finally, the advantage of FT-based method over DB1 and DB2 is shown in Fig. 20.

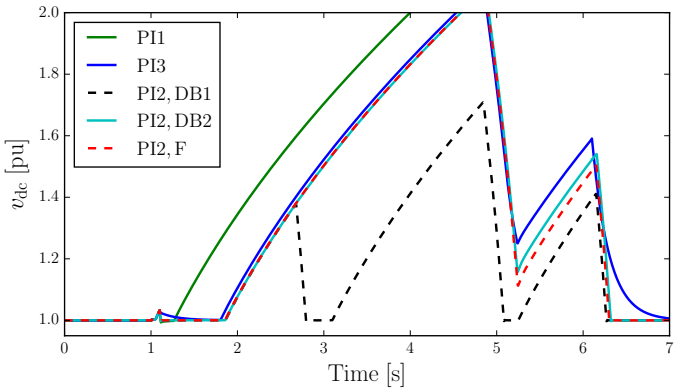

Fig. 19: Scenario I: Response of the DC voltage.

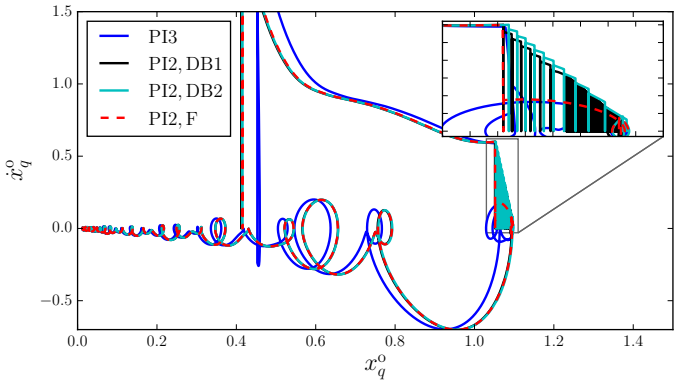

Fig. 20: Scenario I: Time derivative of the integrator state variable with respect to the state variable of the AC voltage controller.

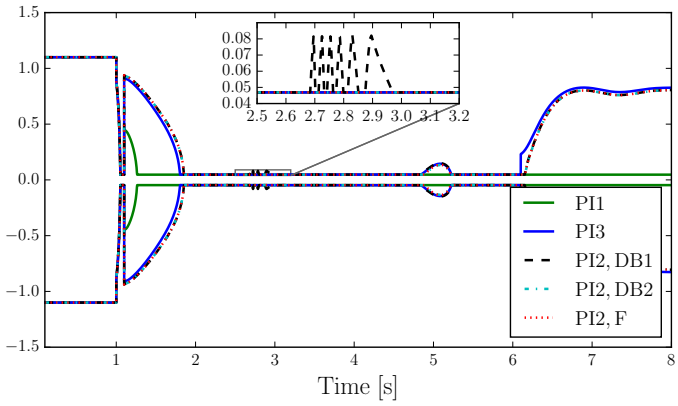

Fig. 21: Scenario II: Response of the $\pm\sqrt{i_{\max}^2 - i_{\mathrm{ac},q}^2}$.

2) Scenario II: This scenario considers a lower value for i_q^{lm} than the maximum current (see Table III). The dynamic response of the $\pm\sqrt{i_{\max}^2 - i_{\mathrm{ac},q}^2}$ and the DC voltage are shown in Figs. 21-22 respectively for the considered PIs. In this scenario, the limits of the d-axis controller do not reach to zero and that is why the v_{dc} response shows a drastically different response compare to the Scenario I. In addition, the delayed response of the PI1 models does not significantly impact the v_{dc} voltage trajectory (see Fig. 22).

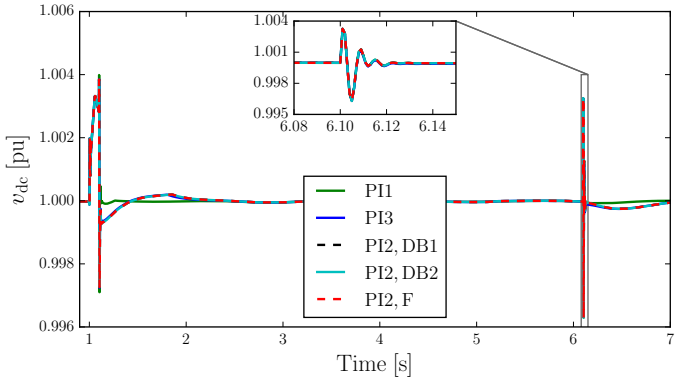

Fig. 22: Scenario II: Response of the DC voltage.

Comparing AW methods, the PI2 and PI3 models show similar v_{dc} because of availability of d-axis current. However the PI2 model with DB1 chattering is observed in the output and thus in the limits and for DB2 only in the output. On the other hand, FT-based model gives raise to smoother trajectories compared with other implementations.

V. Conclusions

This paper proposes two implementations of the IEEE Std. 421.5-2016 conditional AW PI model to consider variable limits. The first implementation is based on a theoretical approach provided by Filippov and the second one is a dead-band based heuristic approach. The dynamic behavior of these models are compared considering two different deployments of outer level configurations coupled with the current limit block of VSCs. Simulation results indicate that each configuration of upper level and limiting technique of PIs have a significant impact on numerical simulation and overall systems dynamic response. Among the available implementation techniques for the Std. AW PI limiters, the proposed theoretical approach provides the most accurate results.

Future work will further extend this work to study the impact of the AW PI implementations with variable limits considering other VSC applications for example, storage, wind generators, smart transformers and micro-grids. It will be also interesting to study the behavior of the proposed technique when coupled with more sophisticated PI controllers, for example the PIs coupled with observer-based controllers that help avoid [2] or mitigate [3], [4] the effect of anti-windup limiters.

Appendix A
Filippov Theory [20]

Consider the following switched dynamical system:

$$R^- : \ \dot{x} = f_1(x), \quad h(x) < 0 \ , \tag{9}$$
$$R^+ : \ \dot{x} = f_2(x), \quad h(x) > 0 \ , \tag{10}$$

with $x \in \mathbb{R}^n, f_1$ and $f_2 \to \mathbb{R}^n, h : \mathbb{R}^n \to \mathbb{R}$, where the switching surface Σ is defined as,

$$\Sigma := \{x \in \mathbb{R}^n : h(x) = 0, h : \mathbb{R}^n \to \mathbb{R}\} \ . \tag{11}$$

Let $r_1(x) = h_x^T(x) f_1(x)$ and $r_2(x) = h_x^T(x) f_2(x)$. Then $x \in \Sigma$ is a crossing point, sliding point of (9)-(10) if

$$\text{crossing} : r_1(x) r_2(x) > 0 \ , \tag{12}$$
$$\text{sliding} : r_1(x) r_2(x) < 0 \ , \tag{13}$$

and an attractive sliding if

$$r_1(x) > 0 \quad \text{and} \quad r_2(x) < 0 \ . \tag{14}$$

At an attractive sliding the solution stays on Σ with a sliding vector filed, as follows,

$$\dot{x} = (1 - \alpha) r_1(x) + \alpha r_2(x) \ , \tag{15}$$

where $\alpha = \frac{r_1(x)}{r_1(x) - r_2(x)}$.

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