Analytic And Numerical Study of TCSC Devices: Unveiling the Crucial Role of Phase-Locked Loops

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***Abstract*—The paper proposes a hybrid dynamic model of thyristor controlled series compensators (TCSCs). The objective is to demonstrate, through advanced circuit theory tools and numerical simulations that some modeling aspects are not properly taken into account in the existing literature. In particular we consider those related to the role of the TCSC impedance when the line current is polluted by harmonics and the phase-locked loops (PLLs). Shooting methods and periodic small signal analyses are utilized to compute the impedance of the TCSC at sub-harmonics that are typical of the sub-synchronous resonance phenomenon. The case study focuses on the impact of sub-harmonics, on the behavior of the TCSC and on the synchronization of the firing angle through the PLL. Modeling recommendations are finally drawn based on the results presented in the paper.**

***Index Terms*—Thyristor controlled series compensator (TCSC), phase-locked loop (PLL), hybrid dynamical systems.**

I. Introduction

A. Motivations

Among flexible alternating current transmission systems (FACTS) devices, thyristor controlled series compensators (TCSCs) are one of the most commonly utilized in practice due to their low costs, relatively simple control and effectiveness to provide series compensation, increase the power transfer capabilities, damp oscillations of transmission systems and reduce the sub-synchronous resonance (SSR) effect [1]. While widely studied, conventional models of TCSCs [2], [3] typically neglect some aspects, i.e., the effects of sub-harmonics on the equivalent impedance of the TCSC and the impact on their dynamic performance of non-ideal phase-locked loop (PLL). This paper attempts to fill this gap and presents a theoretical and numerical analysis of the dynamic behavior of TCSCs. With this aim, the paper exploits recent advances in the formalism and numerical simulation of hybrid dynamical systems that is appropriate to represent the switching nature of FACTS devices.

B. Literature Review

Since the first installed devices in 1991/1992 [4], [5], the interest in TCSCs has steadily grown during the last two decades. In particular, industrial applications have exploited the ability of TCSCs to increase power transfer capabilities of transmission systems and mitigate the SSR phenomenon of conventional power plants coupled to the rest of the grid through long transmission lines. Among theoretical studies on TCSC, we cite [2], [3], [6]–[11]. In recent years, the interest in TCSCs has been renovated by the observation that the control of wind power plants farms can trigger oscillation phenomena similar to the SSR and the insertion of TCSCs proved to be effective to reduce such oscillations [12]–[14].

From a modeling point of view, FACTSs and, thus, TCSCs, are challenging as they mix continuous elements, e.g., inductors and capacitors, as well as discrete elements, e.g., power electronic switches. These models fall in the category of hybrid dynamical systems, which can be described by differential algebraic equations (DAEs) where state variables are reset or where the vector field shows discontinuities (switching) governed by the values of the state variables [15].

The conventional modeling approaches of FACTS devices is defined in [3] and the most accepted TCSC model is formalized in [2]. This paper aims at enhancing the standard TCSC model and focuses, in particular, on two relevant aspects, as follows.

1) Impact of sub-harmonics on TCSC *equivalent impedance:* in the last decade, however, numerical tools to study hybrid dynamical systems have been object of intense study. Some relevant examples are [16]–[19]. In particular, [19] applies the periodic small signal analysis (PAC), largely used in micro-electronics area, whereas [20] extends shooting analysis (SH) to handle hybrid dynamic models.

In this paper, PAC and SH are utilized to determine the impedance of the TCSC as a periodically switched circuit that works in a steady state condition. The focus is on the frequency band of SSR, where the TCSC is expected to have an inductive-type impedance. We show, however, that this requirement might not be satisfied in actual TCSC implementations.

2) Impact of non-ideal PLL*s on the dynamic response of* TCSC*:* the goal is to show how non-perfect synchronization of non-ideal PLLs coupled with polluted currents can reduce the performance of the TCSC control.

Several models of PLLs have been proposed in the literature and implemented in practice. We cite, for example, [21]–[27]. In recent studies, it has been recognized that non-ideal PLLs have a significant impact on the behavior of power electronic converters. For example [28] and [29] discuss the impact of PLL on the small-signal stability of VSC-HVDC converters and type-4 wind turbines, respectively.

To study the impact of real-world PLLs, we apply a controlling technique known as *voltage reversal* [9], [30] aimed at defining the synchronization requirements that need to be satisfied by the firing angle control of TCSCs considering both ideal and real-world PLL models. *Ideal* voltage reversal

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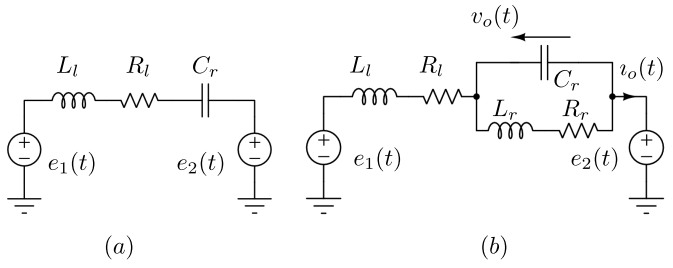

Figure 1. (a) Simplified model of a series compensated line composed of L_l, R_r and the compensating capacitor C_l. The two voltage sources model the generators/areas. (b) The circuit of the improved compensator. The L_r inductor is connected in parallel to the C_r compensating capacitor. The R_r parasitic resistor models losses.

assumes that the voltage across the compensating capacitor is *instantaneously* reversed, i.e., voltage sign is instantaneously changed, when thyristors are turned on. This leads to a square voltage waveform that superimposes to that across the compensating capacitor by integrating the line current. The amplitude of this square waveform can be controlled to regulate the total amount of line compensation.

C. Contributions

The objective of this work is to present an accurate yet readily implementable modeling approach for TCSCs. Main contributions are as follows.

- A thorough discussion based on PAC and SH techniques on the switching behavior of the TCSC, which makes challenging to determine its impedance under different working conditions especially if sub-harmonics are taken into account.
- An in-depth appraisal through the *voltage reversal* technique aimed at defining the synchronization requirements that need to be satisfied by the firing angle control of TCSCs considering both ideal and real-world PLL models.

D. Organization

The remainder of the paper is organized as follows. Section II introduces the basic concepts about series compensation and the basic scheme of the TCSC. Section III presents the proposed hybrid dynamical model of the TCSC based on shooting analysis (SH) and periodic small signal analysis (PAC). Section IV describes the effect of sub-harmonics on the equivalent TCSC impedance and the effect of PLLs on the firing angle synchronization. Numerical results are also presented in this section. Finally, Section V draws relevant conclusions and outlines future work directions.

II. Series Compensation

In the basic circuit shown in Fig. 1(a), the $e_1(t) = E_1 \sin(\omega_o t+\phi_1)$ and $e_2(t) = E_2 \sin(\omega_o t+\phi_2)$ voltage sources represent two generators/areas connected by the line modeled as a series connection of the R_l resistor and L_l inductor. The maximum power transfer between the two generators is obtained by inserting in series to the line the C_l capacitor such that total impedance

$$Z_l(\omega) = R_l + \mathrm{j}\omega\left(L_l - \frac{1}{\omega^2 C_l}\right) \tag{1}$$

is real at $\omega = \omega_o$ which means that the $\omega_l = (L_l C_l)^{-1/2}$ resonance frequency and to ω_o must be made the same. Assume that $e_1(t) = E_1 \sin(\omega_o t + \phi_1) + E_s \sin(\omega_s t)$ and that we would like to "see" an inductive type impedance at $\omega_s < \omega_o$. It is trivial to observe that $\Im\{Z_l(\omega_s)\} < 0$ for $\omega_s < \omega_l$ thus $Z_l(\omega_s)$ being of capacitive type, viz. our target can not be met with the circuit of Fig. 1(a).
Consider the third order circuit in Fig. 1(b) and introduce $\omega_r = (L_r C_r)^{-1/2}$. It also includes a parasitic resistance R_r connected in series to L_r. The resulting equivalent line impedance $Z_l(\omega)$ becomes

$$Z_l(\omega) = R_l + \overbrace{\frac{R_r}{\left(1-\omega^2 L_r C_r\right)^2 + \left(R_r C_r \omega\right)^2}}^{R_{eq}(\omega; R_r, L_r, C_r)} + \mathrm{j}\omega L_l + \mathrm{j}\,\underbrace{\omega \frac{L_r\left(1-\omega^2 L_r C_r\right) - C_r R_r^2}{\left(1-\omega^2 L_r C_r\right)^2 + \left(R_r C_r \omega\right)^2}}_{X_{eq}(\omega; R_r, L_r, C_r)} . \tag{2}$$

Based on the value of R_r, two cases can be distinguished, as follows.

- $\boxed{R_r = 0}$ In this case, $R_{eq}(\omega; 0, L_r, C_r) = 0$ and X_{eq} simplifies as

  $$X_{eq} = \frac{L_r}{1-\omega^2 L_r C_r} \quad .$$

  The $\Im\{Z_l(\omega_o)\}$ becomes equal to 0 when the series resonance frequency

  $$\omega_l = \sqrt{\frac{L_l + L_r}{C_r L_r L_l}} > \omega_r$$

  is equal to ω_o. If $\omega^2 < \omega_r^2$, $X_{eq}(\omega; 0, L_r, C_r) > 0$, thus leading $Z_l(\omega)$ to become of "inductive" type. If $\omega_s^2 < \omega_r^2 < \omega_o^2$, then $X_{eq}(\omega; 0, L_r, C_r)$ is of capacitive type when $\omega > \omega_r$, and particularly at ω_o, and of inductive type when $\omega < \omega_r$ and thus at ω_s. If we assume to vary L_r and keeping C_r fixed, we can adjust the value of X_{eq}. This is important in the sequel.
- $\boxed{R_r \neq 0}$ In this case, observing (2), it follows that $R_{eq}(\omega; R_r, L_r, C_r) \neq 0$. More importantly, if $C_r R_r^2 > L_r$, it follows that $X_{eq}(\omega; R_r, L_r, C_r) < 0$ for $\omega < \omega_r$. In other words, a too high R_r once more does not allow us to meet the target.

Hence, if $R_r = 0$, the circuit shown in Fig. 1(b) properly compensates the inductive reactance of the line at the fundamental frequency $\omega_o = 2\pi f_o$, and "shows" an inductive-type impedance at frequencies (sub-harmonics) where the SSR phenomenon may take place. However, if $R_r \neq 0$, at the harmonics relevant for SSR, the equivalent impedance does not behave as an inductive load but, rather, as a resistive-capacitive one. This discussion allows concluding that losses have to be

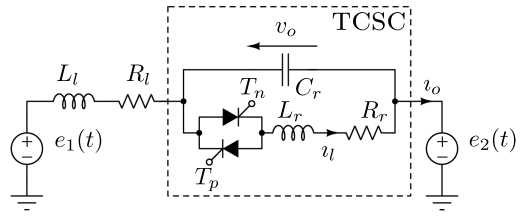

Figure 2. The basic schematic of the TCSC compensator.

carefully considered when studying the circuit of Fig. 1(b). This remark will be crucial for the modeling of the TCSC.

The TCSC circuitry is conceptually similar to the circuit of Fig. 1(b) but has the ability to vary the amount of compensation, i.e. the value of X_{eq}. As anticipated this can be achieved by varying L_r through the circuit shown in Fig. 2. The thyristors T_p and T_n are suitably turned on during each period of the fundamental frequency f_o, thus causing the insertion of the L_r inductance for a fraction of the period. If the thyristors are never turned on, this is equivalent to $L_r = \infty$, whereas, if the thyristors are always conducting, the TCSC behaves as the circuit in Fig. 1(b). Thus it seems that the action of the thyristors modulates the equivalent value of L_r "inserted" in the circuit.

It is important to note that, even if $R_r = 0$, owing to the switching (nonlinear) nature of the circuit, it is not ensured that L_r sinks energy with current "in phase" with the $v_o(t)$ voltage and releases energy with current not "in phase" with $v_o(t)$. As for the circuit of Fig. 1(b), this can deeply change the imaginary part of the equivalent impedance and, mostly important, the TCSC equivalent impedance may exhibits a *resistive* component, even if losses are low by design (i.e., even if R_r is small). It will be shown in the remainder of the paper that this effect is not necessarily a drawback and can actually be beneficial for the dynamic behavior of the TCSC.

III. Hybrid Dynamic Model of the TCSC

A simplified model of the TCSC and of the transmission line to which it is connected can be defined by assuming that the TCSC is driven by an independent current source and that thyristors are characterized by a resistance R_{on} when on and R_{off} when off. These assumptions lead to the following equations:

$$\begin{cases} C_r \dot{v}_o(t) + \imath_l(t) - \imath_o(t) = 0 \\ L_r \dot{\imath}_l(t) + \left(z(t)R_{\text{on}} + (1 - z(t))\, R_{\text{off}} + R_r\right) \imath_l - v_o(t) = 0 \end{cases} \tag{3}$$

where $z(t)$ is a piecewise constant function whose value is set to 1 for $t = \left(\frac{\pi}{\omega_o} - \delta\right)(k+1)$ ($k \in \mathbb{N}$) and to 0 for $t = \hat{t}$ if $\imath_l(\hat{t}\,) = 0$ and $z(\hat{t}\,) = 1$. Furthermore, in (3) $v_o(t)$ is the voltage across C_r, $\imath_l(t)$ is the current through L_r and $\imath_o(t) = A_1 \cos(\omega_o t) + A_s \cos(\omega_s t)$ is the line current, which is assumed to be "polluted" by the component $A_s \cos(\omega_s t)$. This assumption is useful to compute the equivalent impedance at ω_s, similarly to what was done in [2]. The value of L_r must be chosen so that $\omega_r > 2\pi f_o$. Design rules in [3] suggests a X_{L_r}/X_{C_r} ratio in the $[0.1, 0.3]$ range and it is stated that in present installations the used ratio is 0.133 which implies a ω_r resonant frequency of the TCSC equal to about $2.74 f_o$. Moreover, ω_r must not coincide or be close to $2f_o$ or $3f_o$. These rules are followed in the design of the TCSC in [2].

The first two equations in (3) model voltage across C_r and current through L_r. The third equation states that $z(t)$ is constant, but on a discrete set of time instants where it *instantaneously* varies. In a more concise way $z(t)$ is a digital variable that switches between 0 and 1 discrete values at discrete time instants. In these switching time instants the vector field of the second equation in (3) undergoes an instantaneous variation, i.e. the conductance of the thyristors instantaneously switches between R_{on} and R_{off}. It is worth noticing that, owing to the presence of the $z(t)$ digital state variable, the system can be modeled as an hybrid dynamical system and one can exploit the results presented in [31] and [32].

A. Ideal reversal

To understand the TCSC actual behavior, it is useful to study (3) assuming an ideal operating condition first. With this aim, let $R_r = 0$, $R_{\text{off}} = \infty$, $R_{\text{on}} = 0$, $L_r \to 0$, $\delta \to 0$, i.e., the thyristors when on and off behave like short-circuits and open-circuits, respectively. The conduction interval of the thyristors goes to 0 since the resonant frequency $\omega_r \to \infty$. Clearly, these assumptions are unrealistic as, among other issues, the current through the conducting thyristors goes to ∞. With these simplifications, the voltage $v_o(t)$ is the solution of the recursive expression

$$\begin{cases} v_o(t + t_k) = \underbrace{(-1)^{k+1} v_o(t_k)}_{\Xi_k} + \dfrac{1}{C_r} \displaystyle\int_{t_k}^{t_k + t} \imath_o(\tau) d\tau \\ t_k = \dfrac{\pi}{\omega_o}(k+1) \quad , \quad k \in \mathbb{N} \\ t_k < t \leq t_{k+1} \end{cases} . \tag{4}$$

If $A_s = 0$, the integral in (4) gives a null result between t_k and t_{k+1} (peaks of $|\imath_o(t)|$) and $v_o(t_k)$ reverts its sign due to the *instantaneous* oscillation due to the thyristor conduction. The instantaneous capacitor voltage switch is known as *voltage reversal* [9], [30]. The Ξ_k term contributes a square voltage waveform to the solution and the integral part a voltage shifted by $\pi/2$ with respect to the forcing current $\imath_o(t)$ (capacitive impedance). This does not happen if $A_s \neq 0$, as the integral is no longer null along the intervals $[t_k, t_{k+1}]$.

Equation (4) also shows a possible way to control the TCSC, i.e., the thyristors must be turned-on each time the $A_1 \cos(\omega_o t)$ *fundamental* component of the line current reaches a maximum or a minimum. This justifies the π/ω_o term in (3). In turn, this suggests that thyristor turn-on must be synchronized to the fundamental component of the polluted $\imath_o(t)$ line current with a PLL. This crucial aspect of the TCSC modeling is further discussed in the following.

Figure 3 shows the ideal functioning of the TCSC. The voltage $v_o(t)$ (upper trace) exhibits discontinuities and anticipates $\imath_o(t)$ (lower panel) of $\pi/2\omega_o$ due to lower/upper shifting at the maximum/minimum of $\imath_o(t)$. The $v_c(t)$ shifting voltage

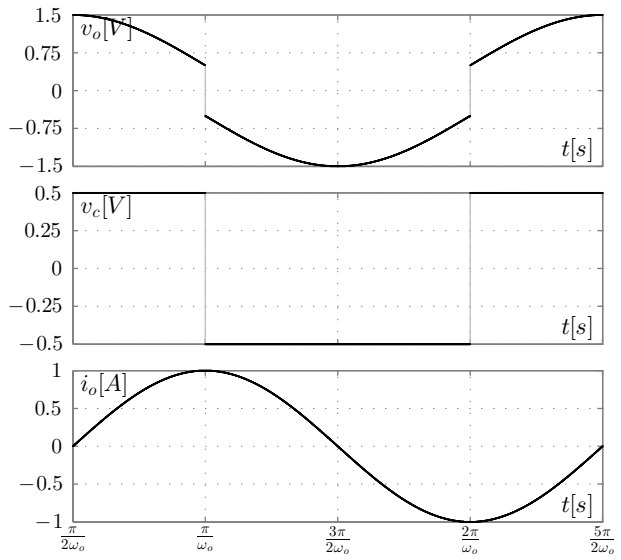

Figure 3. Relevant waveforms of electrical quantities of the TCSC: $v_o(t)$, $v_c(t)$ and $i_o(t)$.

waveform (center panel) is a square wave with zero mean value, in particular

$$v_c(t) = \sum_{k\in\mathbb{N}} \Xi_k \chi_{(t_k,t_{k+1}]}\left(t - \frac{k\pi}{\omega_o}\right) \ , \tag{}$$

where $\chi_{(t_k,t_{k+1}]}(t)$ is the indicator function of the $(t_k, t_{k+1}]$ interval,[2] t_k and Ξ_k are defined in (4).

When the TCSC operates in steady-state, the fundamental component of its Fourier series is a cosine wave whereas the sine component is null.

The impedance of the TCSC working in steady-state conditions can be computed as the ratio between the spectral components of the $v_o(t)$ and $i_o(t)$ periodic waveforms at the same frequency.[3] Hence, the total reactive power by the TCSC depends on the magnitude of the square waveform (at the same magnitude of $i_o(t)$), i.e., it depends on the value of $v_o(t_k)$. This square voltage waveform can be obtained by instantaneously reversing ($\omega_r \to \infty$) the sign of the $v_o(t_k)$ voltage across the C_r capacitor. In practice voltage reversal can be achieved only in a finite amount of time that must not be too short in order to limit the peak value of the $i_l(t)$ current. This suggest to select ω_r as higher as possible while respecting device limits. The $v_o(t_k)$ value can be controlled by anticipating/delaying the reversal time instant along several working periods, thus by departing from a steady state working condition (details are in [3] page 231).

[2]The $\chi_{\mathcal{I}}(x)$ indicator or characteristic function of the generic $\mathcal{I}$ interval is such that $\chi_{\mathcal{I}}(x) = 1$ if $x \in \mathcal{I}$ and $\chi_{\mathcal{I}}(x) = 0$ if $x \notin \mathcal{I}$.

[3]It goes without saying that the use of this impedance is correct only for linear circuits in sinusoidal regime and actually this is not the case. Nevertheless this is a typical "engineering" approach that implies the fact that $A_s \ll A_1$, viz. a sort of small signal (periodic) analysis of the system is performed. This consideration represents an open door towards the analysis presented in the sequel in which PAC is rigorously adopted.

The expression of the Fourier components can be found in closed form if we assume that $\omega_o/\omega_s = n \in \mathbb{N} \setminus \{0, 1\}$. The equivalent impedance at ω_o is as follows:[4]

$$Z(\omega_o) = -\mathrm{j}\frac{4A_s n \tan\frac{\pi}{2n} + 4\omega_o C_r v_o\left(\frac{\pi}{\omega_o}\right) + \pi A_1}{2\pi\omega_o C_r A_1} \ . \tag{5}$$

Equation (5) has the following characteristics:

- $Z(\omega_o)$ does not changes its sign, i.e., it is capacitive and satisfies the TCSC design;
- $Z(\omega_o)$ depends on A_s, i.e., the polluted current acts on the compensation capabilities of the TCSC.
- by dropping A_s, $Z(\omega_o)$ depends *linearly* on $v_o(\pi/\omega_o)/A_1$, where $v_o\left(\pi/\omega_o\right)$ is the instantaneous voltage at the reversal time instant (note that the absolute value of this voltage before and after the ideal reversal is the same).

The latter is an important result that helps the design of the controller. This result was originally derived, although using a different formalism, in [9].

Similarly, the impedance $Z(\omega_s)$ can be obtained as

$$Z(\omega_s) = \frac{\mathrm{j}}{2\pi\omega_s C_r}\left(2n\tan\frac{\pi}{2n} - \pi\right) . \tag{6}$$

The numerator of (6) is always positive and thus leads to an always inductive type impedance at sub-harmonics. This is again, a relevant result. It leads to conclude that the insertion of a TCSC in series to a transmission line achieves the goal to compensate the line at different levels by varying the $v_o(\pi/\omega_o)/A_1$ ratio. Note also that $v_o\left(\pi/\omega_o\right)$ and A_1 do not appear in (6) and this once more is a relevant result: the amount of compensation can be varied without altering the impedance at the sub-harmonics.

Something similar to our investigation on the impedance at the fundamental and sub-harmonics were done in [8], [34], but in these papers the intermodulation effects due to the polluting sub-harmonic were not considered.

The following subsection discusses whether a real design with a current of finite peak value is still adequate to meet the design objectives of the TCSC.

B. Real reversal: impedance determination

Since the TCSC circuit is non-linear, there can be several inter-modulation products that contribute to each impedance value at the discrete set of frequencies. For example this is the purpose of the term A_s introduced in (5).

A possible approach to compute the impedance of the TCSC, which was adopted in [2], is to perform a time domain simulation for a long simulated time, to ensure that the TCSC operates in a periodic steady-state and then to perform Fast Fourier Transform (FFT) to derive the spectra of $v_o(t)$ and $i_o(t)$. The ratio between the corresponding components of the spectra can be considered as the impedances of interest. However, more efficient and accurate results can be obtained by adopting a well-known approach that has been largely applied to micro-electronic circuits. This approach is as follows:

[4]The expressions of $Z(\omega_o)$ and $Z(\omega_s)$ have been derived using Mathematica [33].

- A single SH is performed to accurately determine the periodic solution without any perturbation applied to the circuit.
- Then a small signal source that does not perturb the large signal solution can be added as input and a PAC analysis can be performed to compute the effects of the small signal perturbation, for example the impedance of the TCSC [35], [36].

The SH method solves the $\phi(x_o, t_0, t_0+T)-x_o = 0$ boundary value problem where $x_o \in \mathbb{R}^S$ is the unknown vector of S initial values of state variables at the t_0 time instant, T is the working period of the circuit and $\phi(\cdot)$ is the state-transition function. The $\phi(x_o, t_0, t_0+T)$ vector can be determined with a conventional time-domain analysis along only one T period. This approach is considerably more efficient than performing several time-domain simulations along a large number of T periods until the circuit reaches the steady-state working condition, i.e., satisfies the above boundary condition [35].

PAC allows computing periodic transfer functions as the independent variable is the frequency that is swept in the desired interval. To this aim, PAC linearizes the circuit along the steady state solution found by SH, i.e., it derives what is known as variational model [37]. A periodic small signal is then injected into the variational model of the circuit and its effects are computed. Since the original circuit works on a periodic orbit, the variational model and, hence, PAC can capture intermodulation effects.

It is important to note that, since the TCSC is switched as described in Section III and the turn-off of thyristor depends on the state variables of the circuit (see (3)), the PAC analysis cannot be applied directly because the variational model is not defined at the switching time instants. To deal with hybrid circuits both SH and PAC analyses have to be properly adapted and extended as discussed in [31], [32]. These techniques have been already profitably applied to power circuits and power systems [18]–[20].

In this case, we applied SH to (3) with $A_s = 0$, i.e., with a non-polluted $\imath_o(t)$. Then, PAC is used to compute the effects of a small $A_s\cos(\omega_s t)$ current superimposed to the $\imath_o(t)$ line current, sweeping ω_s in the $2\pi[100\,\mathrm{mHz}, 60\,\mathrm{Hz}]$ interval. For each value of ω_s, the spectral component of the $v_o(t)$ small signal was derived at $\omega = \omega_s$. The ratio between such a component and the injected current gives the equivalent impedance at $\omega = \omega_s$.

As a first example, we consider the circuit described in [2]. The numerical analysis is performed using a circuit simulator that is described in [38]. The design of this TCSC is such that it acts as a capacitive line compensator with the firing angle α that take values in the range $[70^o, 90^o]$. By referring to (3) we have that $\alpha = 180^o(1/2 - \omega_o\delta/\pi)$. Numerical results are shown in Fig. 4. The X_{68} imaginary part of the impedance when $\alpha = 68^o$, i.e., slightly less than the lower design bound, is clearly positive in the sub-harmonic range. For $\alpha = 70^o$, i.e., high line compensation, the imaginary part X_{70} is slightly positive up to about 25 Hz, i.e., inductive in the sub-harmonic range (see Fig. 4). The R_{78} real and the X_{78} imaginary part of the impedance at $\alpha = 78^o$ are shown in Fig. 4. X_{78} is *negative* in the entire frequency range, this means that the behavior of

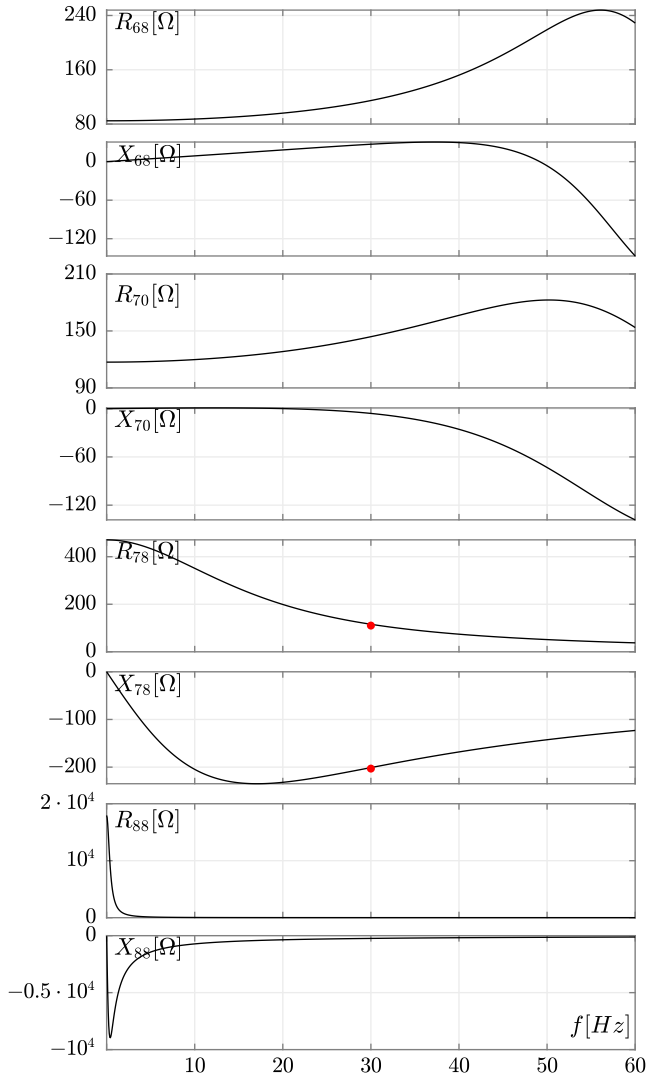

Figure 4. R_α and X_α represent the real and imaginary part, respectively, of the TCSC equivalent impedance computed at the α firing angle (in degree).

the TCSC at sub-harmonics is *capacitive* and not inductive as expected The behavior worsens at $\alpha = 88^o$, i.e., at lower line compensation, since X_{88} is even larger at sub-harmonics.

The effectiveness of the results by the PAC analysis was largely and already proved in several works [19], [36], [38]. Once more to check this, we computed the impedance by considering the polluting signal as a large signal with $\alpha = 78^o$ through the SH analysis performed over the period corresponding to 30 Hz. The impedance was computed through the FFT; the result is the "dots" in the corresponding panels of Fig. 4. The impedance by PAC is $115.77 - 200.98j$ and that by SH is $110.23 - 203.87j$ that are in very good agreement. We recall that PAC is much faster than SH and does not have limitations on the frequency of the small signal tone (the simulation time must be the smallest common multiple of the periods corresponding to ω_o and ω_s).

The PAC analysis reveals that, even within design limits, the TCSC does not always work as expected and that the resistive part of its equivalent impedance is the life line for several

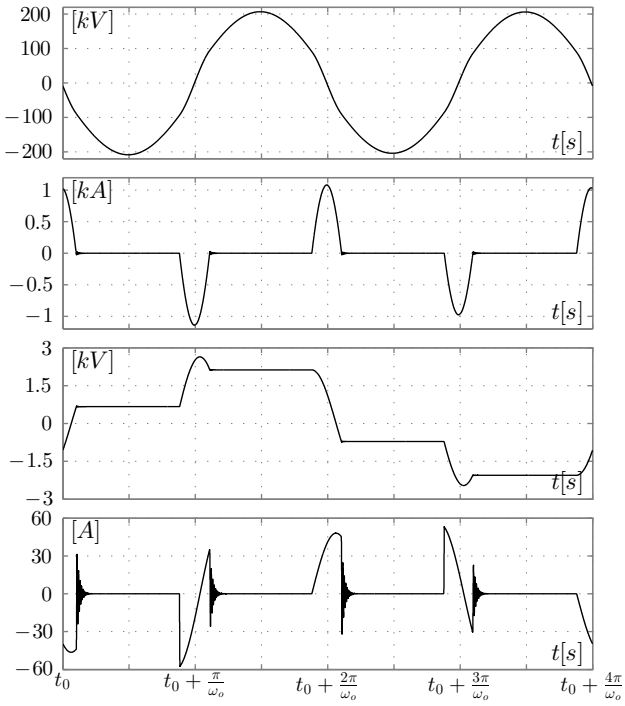

Figure 5. Upper panel: the TCSC voltage with ideal synchronization. Central upper panel: the current across the L_r inductance with ideal synchronization. Central lower panel: the difference between the TCSC voltages obtained with current peak and ideal synchronization. Lower panel: the difference between the currents across the L_r inductance obtained with current peak and ideal synchronization.

values of the α firing angle. The next section discusses another aspect of the TCSC model that has been neglected so far in the literature.

IV. Impact of PLL on the TCSC Behavior

In the SH analysis carried out in Sec. III-B, the TCSC is assumed to be perfectly synchronized with the time instants of the peak values of the current fundamental. In a real implementation of a TCSC, however, the synchronization is achieved through a PLL that locks the firing angle to the f_o component of the $\imath_o(t)$ line current. In the literature, it is generally assumed that the firing angle is synchronous with the peak values of the fundamental (f_o) component of $\imath_o(t)$ in presence of harmonic pollution. However, such a synchronization, i.e., the model of the PLL, should be carefully considered because it has a relevant impact on the design of the TCSC control and its dynamic behavior. The effect of non-ideal synchronization and of the PLL model are thoroughly discussed in the remainder of this section.

A. Non-ideal Synchronization with Polluted Current

In order to define the impact of the PLL model, a SH and PAC analysis are carried out for $\alpha = 68^{\circ}$. In this case, however, the TCSC is synchronized with the peak values of the *polluted* $\imath_o(t)$ current, not with the peaks of the fundamental component of the current at f_o. Results are shown in Fig. 5. For comparison, Fig. 5 also shows the results obtained by correctly synchronizing the TCSC on the peak values of the fundamental harmonic of $\imath_o(t)$. The $v_o(t)$ voltages and the currents flowing through the L_r inductor in the case of perfect synchronization and peak synchronization are reported in the two upper panels of Fig. 5. Differences between the ideal and the actual trajectories are shown in the two lower panels; they are exclusively due to the different times at which thyristors are turned on. While small, such differences have a non-negligible impact on the resulting TCSC equivalent impedance.

Figure 6 shows the impedance of the TCSC for $\alpha = 68^{\circ}$ computed through the PAC analysis when it is synchronized with the peak value of the polluted $\imath_o(t)$. In the same figure these results are compared with those previously obtained for perfect synchronization and already shown in Fig. 4. The large differences in the real and imaginary parts of the impedance can be easily appreciated. The real part of the impedance increases when the TCSC is synchronized to the peak values of the polluted $\imath_o(t)$ current. From the observation of the imaginary parts, it is also evident that the inductive-type mode is completely "lost".

B. Time-Domain Analysis with PLL

For completeness and comparison, we have also computed the impedance of the TCSC model discussed in [2] without adopting the PAC analysis. With this aim, we performed a time-domain analysis with fixed firing angle for $20\,\mathrm{s}$ of simulated time, by using the model in [2] that was implemented in SIMULINK. The need for such a "long" time-domain integration, is to be able to assume that the circuit is in stationary conditions, since SIMULINK that does not implement any steady-state analysis. Then, the spectrum of $v_o(t)$ and $\imath_o(t)$ were computed through a FFT on the evenly time spaced samples in the $[19\,\mathrm{s}, 20\,\mathrm{s}]$ interval with a sampling rate $1/50\,\mu\mathrm{s}$. A $1\,\mathrm{s}$ interval ensures a frequency resolution of $1\,\mathrm{Hz}$. The impedances are reported in Table I.

The most relevant observation that can be drawn from this table is that $Z(30)$ is always largely capacitive. This result is in contrast with the result shown in Fig. 4 and is a direct

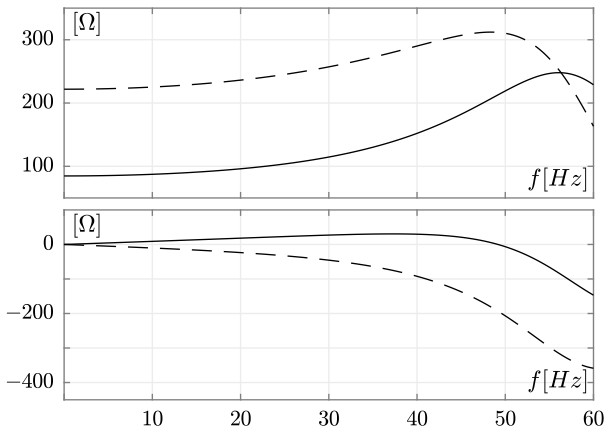

Figure 6. For $\alpha = 68^{\circ}$, real part and imaginary part of the TCSC equivalent impedance (upper and lower panels, respectively). Solid curves refer to ideal synchronization and dashed ones to peak synchronization.

Table I
THE IMPEDANCE AT 30 Hz AND 60Hz OF THE TCSC DESIGN IN [2].

α	$Z(60)$	$Z(30)$
70°	$0.256 - 153.22\text{j}$	$189.382 - 60.75\text{j}$
78°	$-0.183 - 125.48\text{j}$	$93.157 - 171.99\text{j}$
88°	$0.071 - 120.15\text{j}$	$-0.265 - 240.33\text{j}$

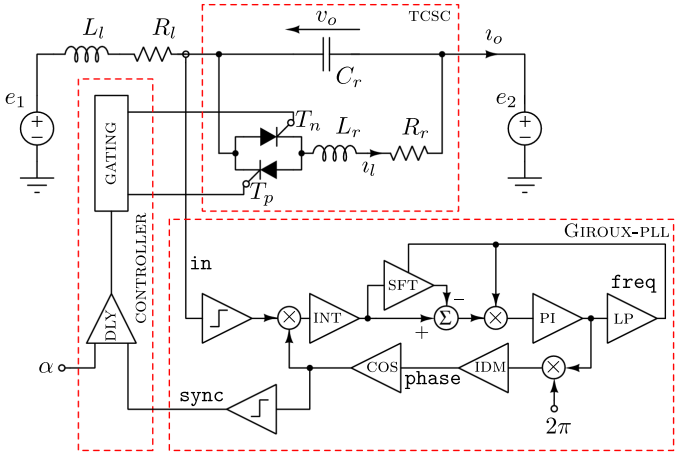

Figure 7. The schematic of the TCSC synchronised by the second-order digital PLL. $R_l = 6.0852\,\Omega$, $L_l = 0.4323\,\text{H}$, $C_r = 21.977\,\mu\text{F}$, $L_r = 43\,\text{mH}$, $R_{\text{on}} = 10\,\text{m}\Omega$, $R_{\text{off}} = 1\,\text{G}\Omega$, $e_1(t) = 539\,\text{kV}\sqrt{2/3}\sin(120\pi t) + V_s\sin(\omega_s t)$, $e_2(t) = 477.8\,\text{kV}\sqrt{2/3}\sin(120\pi t - 0.066549)$. V_s sets the amount of "pollution".

consequence of the imperfect synchronization of the TCSC firing angle obtained with the non-ideal PLL model [26].

It is now clear that the PLL plays an important role in the design of the TCSC. For polluted currents, in fact, a non-perfect synchronization with the fundamental component of $\imath_o(t)$ leads to unexpected dynamic behavior of the TCSC.

C. *Effect of Different* PLL *Designs*

To complete our investigation, we considered several PLLs [21]–[27]. We started by inserting in the TCSC model the same PLL used in [2]. The (block) schematic of this single-phase version of the TCSC is shown in Fig. 7. The value of the parameters of the circuit elements are reported in the figure caption. The circuit is composed of three main parts: the TCSC, which is the same circuit of [2], the CONTROLLER that drives the thyristors and the PLL that delivers the `sync` signal to the controller. The PLL is described in [26] and is often chosen for its superior characteristics and robustness. This PLL model, however, is mainly utilized in theoretical studies as it cannot be easily implemented in practice [27]. Its main blocks are: INT that implements an ideal integrator; LP that implements a second-order low-pass filter; PI that implements a proportional-integral block, IDM that performs a modulus integration, i.e. any time the output value goes above an upper threshold (in this case 2π) the integrator is reset to 0; SFT that replicates its input waveform with a delay equal to $1/\texttt{freq}$ and finally the COS block that generates an output signal which is the cosine of its input (local controlled oscillator (LCO)). Note that we implemented the PLL through behavioural digital

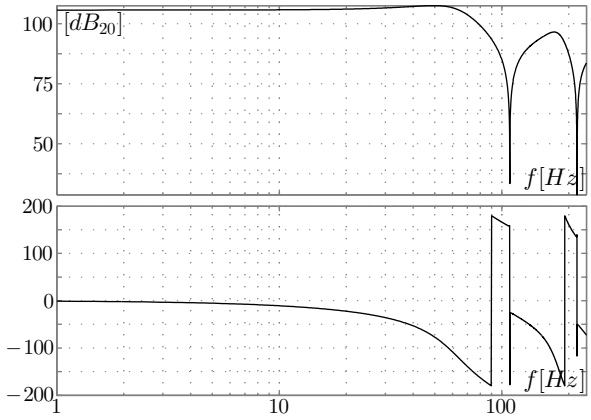

Figure 8. Upper panel: modulus of the transfer function between the TCSC voltage and the synchronization voltage. Lower panel: the phase of the transfer function.

or analog blocks by using advanced description languages such as VERILOG and VERILOGA. The same applies to the CONTROLLER block and thyristors.

An accurate and careful analysis of this PLL model reveals that it is not able to completely remove the polluting components that cause jitter of the input signal with respect to the signal generated by the local oscillator COS block). It is an analog PLL; the output of the analog input multiplier is filtered by integrating it along a time moving window of length equal to the current period of the LCO frequency. By referring to Fig. 7 this task is performed by the INT block, the two multipliers, the SFT block and the adder. This integration is equivalent to a comb-filter whose zeros are at multiples of the LCO frequency. This means that the polluting components are not completely filtered out since they do not fall at any zero of the filter. An adequate locking speed of the PLL is obtained by varying the time aperture of the window. The incomplete removal of the jitter reflects in the PLL output and thus leads to an imperfect synchronization and to the impedance issues described above. Fig. 8 shows the transfer function between the synchronization signal that drives the TCSC and the $v_o(t)$ voltage as obtained through the PAC analysis. The figure shows that there are no poles up to about 60 Hz and that the gain is very large, i.e., more than $100\,\text{dB}_{20}$. The transfer function is parametrized with the firing angle α but the high gain is preserved. This means that even a very small variation of the synchronization provided by the PLL leads to a very large variation of $v_o(t)$ and thus of the impedance of the TCSC.

Finally, we considered the PLL described in [23], which shows *a more appropriate synchronization scheme for* TCSC. *Simulation results show that it has better performance* [22]. This SOGI-FLL is based on a high-q band-pass filter, its name is the acronym of "second order generalized integrator" that exhibits a null phase-shift at center frequency. Its (block) schematic is shown in Fig. 9. The center frequency is adapted by the PLL loop. Locking speed is achieved by adapting the filter center frequency and good performance is achieved by the high-q filter. Despite these properties, the SOGI-FLL does not attenuate the polluting component at 30 Hz of $100\,\text{dB}_{20}$

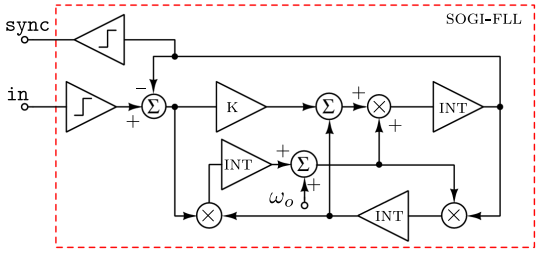

Figure 9. The schematic of the SOGI-FLL.

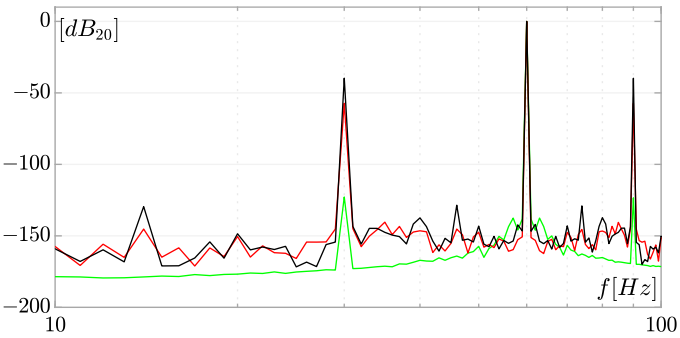

Figure 11. Spectra of the output signals of the different PLLs used in a TCSC working in a steady state condition with a polluted $i_o(t)$ current. The black curve refers to the PLL described in [26]; the red curve to the SOGI-FLL described in [23]; the green curve refers to second order digital PLL described in [39].

and, once more, it appears to be inadequate to synchronize the TCSC and to meet the TCSC impedance requirements.

The results obtained above suggest that a possible strategy to attenuate the polluting components is to reduce as much as possible the bandwidth of the PLL, i.e. to largely filtering the line current. This strategy can introduce a severe limitation in the design of the controller of the TCSC since its speed may be consistently reduced. For example, we tested the second-order digital PLL based on a three-state phase-frequency detector with a bandwidth of 1 Hz as described in [39]. The (block) schematic is shown in Fig. 10. The FF1 and FF2 blocks implement the RS-FLIP-FLOPs of the phase-frequency detector. The output signals drive the charge-pump (CP) implemented by the voltage controlled current sources, which sink/source the $i_{\rm cp}$ current. The current by the CP drives the low-pass filter (LP). The voltage of the LP constitutes the error signal of the voltage controlled oscillator (VCO) that synchronises to $i_o(t)$. The cut-off frequency of the LP sets the bandwidth of the PLL. This PLL model proved to work well as it allows the TCSC meeting the impedance requirements, but the bandwidth is severely limited. This makes the TCSC slow if controlled to damp oscillations of transmission systems.

Fig. 11 shows the spectra of the output signals of the three PLL models considered so far. The comparison is drawn for a TCSC working in steady-state with a polluted $i_o(t)$ current. As it can be seen, at 30 Hz the more attenuated components are those by the digital PLL proposed in [39]. Being below -100dB_{20} and considering the magnitude of the transfer function between the TCSC voltage and the output of the PLL shown in Fig. 8, they do not cause any appreciable effect in the impedance of the TCSC.

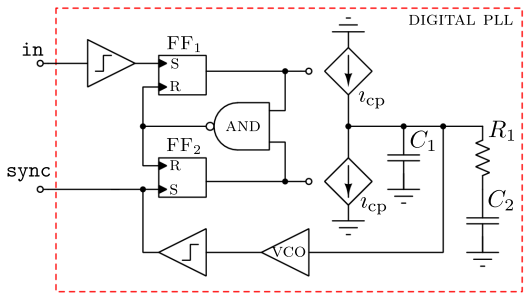

Figure 10. The schematic of the second-order digital PLL. $C_1 = 1.59\,\text{mF}$, $C_2 = 0.17\,\text{mF}$, $R_1 = 1\,\text{k}\Omega$, $i_{\rm cp} = 12.02\,\text{mA}$, $k_{\rm vco} = 2$.

D. *Remarks on* PLL *Design for* TCSC *Control*

Based on the simulation results discussed so far, the following concluding remarks are relevant.

- The impedance of the TCSC is *strictly* related to the architecture of the controller. The synchronization of the controller with the line current is a crucial aspect of the controller. Thus, the PLL is a key element of the whole TCSC design.
- If the PLL is unable to correctly drive the TCSC controller, at sub-harmonics the equivalent impedance of the TCSC is of resistive/capacitive type and makes the design less robust.
- The PLL should be as fast and as immune from pollution of line current as possible. Any phase or time shifting of the reference signal generated by the PLL with respect to the line current impacts on the delay time used to suitably trigger the thyristors in the TCSC. This delay modulates the effects of the L_r inductor and largely modifies the impedance of the TCSC.

V. Conclusions

The paper exploits recently developed analytic and numerical techniques for the analysis of hybrid dynamic systems such as shooting analysis (SH) and periodic small signal analysis (PAC) to study the behavior of thyristor controlled series compensator (TCSC) devices. The paper shows that the TCSC equivalent impedance at sub-harmonics is consistently different from the impedance at the fundamental frequency. The paper also thoroughly discusses the impact of the design of the PLLs on the dynamic response of the TCSC controller and indicates the features that PLL should have to minimize such impact.

Future work will focus on the definition of a TCSC model that is both accurate enough to take into account the impact of sub-harmonics and PLL devices and adequate for transient stability analysis of power systems. Such a model will allow to study accurately the effect of TCSC devices when coupled with large power systems models.

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