Impact of PLL frequency limiter on Synchronization Stability of Grid Feeding Converter

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***Abstract*—It is well known that grid-feeding converters that synchronize to the grid through a Phase-Locked Loop (PLL) can become unstable after a fault. An often-neglected element that plays an important role in the converter synchronization stability is the PLL frequency limiter. While it slows down the phase change during the fault, the frequency limiter also constrains the error of the PLL input, thus leading to a longer settling time. This letter investigates the mechanism of the converter synchronization stability caused by the frequency limiter and provides a taxonomy to evaluate its impact on the overall system dynamic response.**

***Index Terms*—Synchronization stability, grid-feeding converter, Phase-Locked Loop (PLL), Frequency Limiter (FL).**

I. Introduction

Loss of synchronization in the presence of the fault is one of the main concerns for grid-feeding converters [1]. In a weak grid, the converter acts as a positive feedback loop with respect to its own synchronization process, thus worsening the stability of the grid. During a severe low-voltage condition, the converter may lose its synchronization even if the fault ride through requirement is satisfied and this instability may continue even after the fault is cleared [2].

Grid-feeding/following converters use a Phase-Locked Loop (PLL) for the synchronization and aim to inject the assigned power or current into the grid. To capture the synchronization transients, reference [3] proposes a Quasi-Static Large-Signal (QSLS) model. Although the current transients can worsen the synchronization stability [4], the inclusion of the feed-forward compensator in the converter current control can alleviate this negative impact and ensure the accuracy of the QSLS model [5]. To compute the critical cleaning time, based on the QSLS model, reference [6] proposes an Equal Area Criterion (EAC) method and reference [7] proposes a phasor portrait method.

However, to the best of our knowledge, no previous literature investigates the mechanism of the converter synchronization stability caused by the frequency limiter (FL), which is generally applied in the PLL control loop in reality to avoid an excessive frequency mismatch with the grid. After the frequency is saturated, the transient phase movement is solely dependent on the value of the FL. During a severe fault, on the one hand, the converter transient frequency hits the limit, which constrains the speed of the phase change benefiting the stability; on the other hand, the restricted frequency also limits the error of the PLL controller and this will increase the settling time worsening the stability. Therefore, the inclusion of the FL in the PLL has a very significant impact on the mechanism of the synchronization stability and affects the stability assessment, and is therefore worth studying in detail. This letter analyzes this synchronization mechanism and provides a taxonomy for all kinds of faults.

II. Quasi-Static Large-Signal Model

Figure 1 shows the control structure of the grid-feeding converter, where the grid-feeding converter detects the voltage at the point of common coupling (PCC) by a general synchronous reference frame PLL (SRF-PLL) and controls the output current to track its reference i_d^*, i_q^*. The feed-forward compensator in the current control can decouple the current control from the grid side and stabilize the current in milliseconds. Then the converter can be seen as an ideal current source. Assuming the PCC voltage is the reference with the phase at 0 rad, then the PCC voltage in the q-axis can be obtained [4].

$$v_q = r_g i_q^* + \omega l_g i_d^* - V_g \sin(\delta) \tag{1}$$

When the phase is locked ($v_q = 0$), the synchronization is realized. The PI controller of the PLL is used to force the v_q to be null, the dynamics for which are governed as follows:

$$\frac{d\Delta\omega}{dt} = K_p \frac{dv_q}{dt} + K_i v_q \tag{2}$$

$$\frac{d\delta_{pll}}{dt} = \Delta\omega \tag{3}$$

Equations (1)-(3) define the conventional QSLS model utilized for the synchronization stability analysis as shown in Fig. 2.

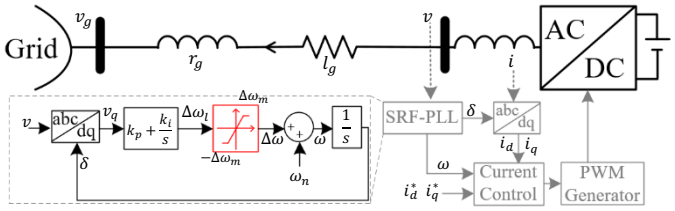

Fig. 1. Grid-Feeding Converter system structure

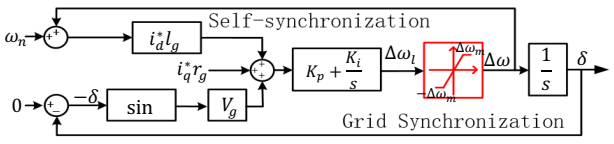

Fig. 2. Grid-Feeding Converter Quasi-Static Large-Signal Model

III. Taxonomy of PLL Frequency Limiter Impact

A FL is generally implemented in a PLL to restrict the error accumulated in the PI control, and more importantly, to avoid an excessive frequency mismatch with the grid, as follows:

$$-\Delta\omega_m \le \Delta\omega \le \Delta\omega_m \quad (4)$$

If the equilibrium point exists during the fault, the FL restricts the error and prolongs the settling time; while if there is no equilibrium point, this limiter suppresses the change rate of the phase as indicated in (3), and allow more time to clear the fault. Accordingly, the impact of the FL on the synchronization can be classified in two situations, namely, with or without equilibrium points, as discussed below.

A. With Equilibrium Point

Figure 3 shows the movement of the phase δ with respect to $-v_q$. Initially, the grid voltage is $V_{g,0}$ and the converter stabilizes at δ_0. When the grid voltage sags to $V_{g,s}$, there are two equilibrium points: one is stable at $\delta_s = \sin^{-1}\frac{r_g i_q^* + \omega_n l_g i_d^*}{V_{g,s}}$ and the other is unstable at $\delta_u = \pi - \sin^{-1}\frac{r_g i_q^* + \omega_n l_g i_d^*}{V_{g,s}}$. At the instant of the fault, v_q step changes to $(V_{g,0} - V_{g,s})\sin(\delta_0)$ with unvaried phase. This activates the proportional channel of the PI controller, and hence, the converter frequency deviation at t_0 is given by:

$$\Delta\omega(t_0) = \frac{K_p(V_{g,0} - V_{g,s})\sin\delta_0}{1 - K_p l_g i_d^*} \quad (5)$$

If $\Delta\omega(t_0) > \Delta\omega_m$, the FL suppresses the converter frequency at $\Delta\omega_m + \omega_n$. Then, the frequency transient before the FL is given by:

$$\Delta\omega_l(t_0) = K_p(\Delta\omega_m l_g i_d^* + (V_{g,0} - V_{g,s})\sin\delta_0) \quad (6)$$

with $\Delta\omega(t_0) > \Delta\omega_l(t_0) > \Delta\omega_m$. After the fault occurrence, since $v_q > 0$, the phase increases along with the red line in Fig. 3 and v_q reduces. After the phase increases beyond δ_s, although v_q becomes negative, $\Delta\omega$ is still positive due to the integral part of the PI control. If $\Delta\omega(t)$ crosses zero before the phase reaches δ_u, the phase will reduce and converge to δ_s. Otherwise, the converter losses synchronization. During this process, $\Delta\omega(t)$ is monotonically decreasing and the phase is the integral of $\Delta\omega(t)$ up to the time as shown in Fig. 3, where t_1 is the time that $\Delta\omega(t)$ takes to decrease to $\Delta\omega_m$ in the case without FL ($\Delta\omega(t_1) = \Delta\omega_m$), t_2 is the time that $\Delta\omega_l(t)$ takes to decrease to $\Delta\omega_m$ in the case with FL ($\Delta\omega_l(t_2) = \Delta\omega_m$) and t_3 is the time that the phase of the two cases cross, the value of which can be computed from the equivalent area (A_1=A_2):

$$\int_{t_0}^{t_1}(\Delta\omega_l(t) - \Delta\omega_m)dt = \int_{t_1}^{t_2}(\Delta\omega_m - \Delta\omega(t))dt + \int_{t_2}^{t_3}(\Delta\omega_l(t) - \Delta\omega(t))dt \quad (7)$$

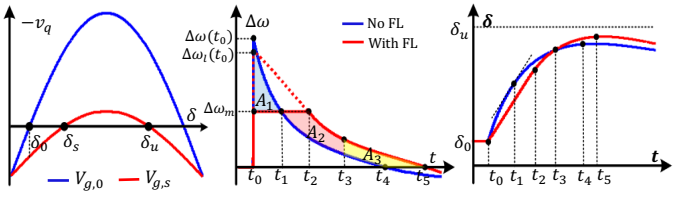

Fig. 3. Phase movements at the situation of equilibrium point existed.

Note that t_3 is the critical time at which the transient phase of the PLL with FL becomes larger than that without FL. The smaller $\Delta\omega_m$, the larger t_3. When the frequency deviation decreases to zero ($\Delta\omega(t_4) = \Delta\omega_l(t_5) = 0$), the phase of the case with FL is larger than that without FL, $\delta(t_4) < \delta(t_5)$, the area of which is A_3. If $\delta(t_4)$ is the critical angle δ_u, then $\delta(t_5)$ is an unstable point. Hence, the inclusion of the FL worsens the synchronization stability in the situation that an equilibrium point existed during the fault with $\Delta\omega_m < \Delta\omega(t_0)$. Particularly, the smaller $\Delta\omega_m$, the larger A_1 resulting in a longer t_3 and a worse synchronization stability.

Note that if an anti-windup strategy is implemented in addition to the FL, the PI controller would not accumulate the error after the saturation and then would withdraw the saturation faster between t_1 and t_2, depending on the anti-windup strategy. Consequently, the area of A2+A3 would be smaller and the peak phase during transients would be smaller than the PLL without anti-windup. Thus, the inclusion of anti-windup limiters can help alleviate the negative effect of the FL on the synchronization stability. However, different anti-windup strategies have different algorithms for dealing with the saturation [8] and would therefore have different effects on the synchronization transients. A detailed analysis of these different strategies is beyond the scope of this letter and needs a further in-depth analysis.

B. Without Equilibrium Point

Now the grid voltage sags to $V_{g,u}$ with no equilibrium point. v_q in transient is always positive so that δ keeps accelerating. If $V_{g,u}$ is not too small, before 90°, the increased phase decreases v_q, $\Delta\omega$ at first may reduce until the phase exceeds 90° or the integral part of the PI control becomes dominant as shown in Fig. 4. If $V_{g,u}$ is very low, e.g. 0 pu, the integral part of the PI control is dominant at the beginning and then $\Delta\omega$ increases with time as shown in Fig. 5. Whether $\Delta\omega(t)$ increases or decreases after the fault occurrence can be identified via $\Delta\dot{\omega}(t_0)$, the value of which is:

$$\Delta\dot{\omega}(t_0) = \frac{K_p l_g i_d^* \Delta\omega(t_0) + K_p(V_{g,0} - V_{g,s})\sin\delta_0 - V_{g,s}\cos(\delta_0)\Delta\omega(t_0)}{1 - K_p l_g i_d^*} \quad (8)$$

where $\Delta\omega(t_0)$ is the frequency deviation at the instant of the fault, which can also be computed in (5). $\Delta\omega(t)$ tends to increase with the time; when its value is over than $\Delta\omega_m$, the phase will increase faster than that with FL. Hence, the FL slows down the increase in phase, which gives more time to clear the fault before the phase reaches an unstable region. There are several conditions in relation to the fault voltage $V_{g,u}$:

a) If $\Delta\omega_m > \Delta\omega(t_0)$, as shown in Fig. 4, t_1 is the time at which $\Delta\omega(t_1) = \Delta\omega_m$. If the fault is cleared before t_1, then whether FL is implemented or not has no effect on the synchronization; if the fault is cleared after t_1, then the inclusion of the FL can improve the synchronization stability by slowing down the phase increase.

b) If $\Delta\omega_m < \omega(t_0)$ and $\Delta\dot{\omega}(t_0) > 0$, the FL slows down the phase increase from the instant of the fault, thus, it can improve the synchronization stability.

c) If $\Delta\omega_m < \omega(t_0)$ and $\Delta\dot{\omega}(t_0) < 0$, as shown in Fig. 5, the transient response before $\Delta\dot{\omega}(t_0) = 0$ is similar with the case with equilibrium points (Fig. 3). If A_1<(A_2+A_3), there will be a time t_3 that the transient phase is the same for the converter with and without FL as indicated before in (7). Then, in the period t_3~t_6, the phase of the converter with FL is larger than without FL, whose value can be computed from equivalent area in Fig. 5 (A_3=A_4):

$$\int_{t_3}^{t_4}(\Delta\omega(t)-\Delta\omega_l(t))dt+\int_{t_4}^{t_5}(\Delta\omega_m-\Delta\omega(t))dt=\int_{t_5}^{t_6}(\Delta\omega(t)-\Delta\omega_m)dt \quad (9)$$

Where t_4 is the time that $\Delta\omega_l(t)$ takes to increase to $\Delta\omega_m$, t_5 is the time that $\Delta\omega(t)$ takes to increase to $\Delta\omega_m$. After t_6, the converter with FL has a worse transient response. From Fig. 5 and analysis in section III-A, it can be deduced that the decrease in $\Delta\omega_m$ enlarges the area of A_1, shrinks the period of $t_2 \sim t_4$ and prolongs t_3. Until $A_1 > (A_2+A_3)$, the phase of the converter without FL is greater than that with FL from the instant of the fault.

Therefore, the inclusion of the FL can improve the synchronization stability and the lower $\Delta\omega_m$ the higher the stability. Note that the inclusion of the anti-windup limiters can speed up the saturation withdrawal, which, in turn, can help stabilize the converter after the fault clearance.

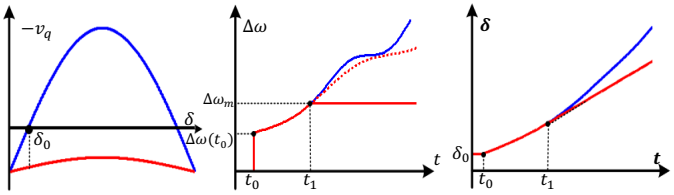

Fig. 4. Phase movements at the situation of $\Delta\omega_m < \omega(t_0)$ and $\Delta\dot{\omega}(t_0) > 0$.

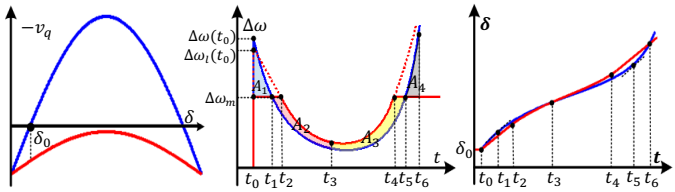

Fig. 5. Phase movements at the situation of $\Delta\omega_m < \omega(t_0)$ and $\Delta\dot{\omega}(t_0) < 0$.

IV. Validation Example

A time-domain EMT simulation solved in Matlab/Simulink is used to verify the analysis on the effect of the FL on the synchronization stability. A 10 kV, 1 MW grid-feeding converter connected to a 50 Hz grid through an 0.12 H L-filter and a $l_g = 0.1\ H, r_g = 1\ \Omega$ transmission line is discussed. The converter setpoint is $i_q^* = 81.65\ A;\ i_q^* = 0$. The PLL PI parameter is 0.022/0.392 and the current controller PI parameter is 1200/2433. There are three scenarios under the consideration corresponding to Fig. 3~5.

Fig. 6 shows the results of the frequency change and phase response after a voltage sag to from 1pu to 0.35 pu at 5 s corresponding to the condition where equilibrium points existed. In this situation, the inclusion of the FL worsens the synchronization stability. The lower the FL value, the larger A_1 area in Fig. 3 and the longer t_2 and t_3. The FL leads the phase to exceed the critical point but $\Delta\omega$ does not fall to zero, as consequence the converter loses synchronization stability.

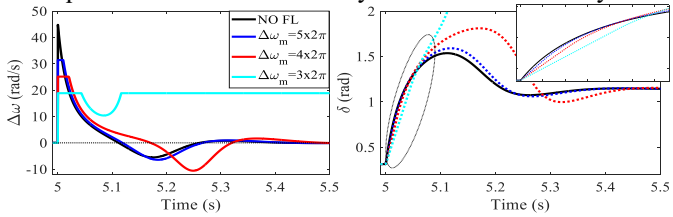

Fig. 6. Results in the situation of equilibrium points existed.

Figure 7 shows the results in the situation of a voltage sag to 0.1 pu at 5 s and recovery at 5.05 s corresponding to the situation of no equilibrium point with $\Delta\dot{\omega}(t_0) > 0$. Without FL, the converter loses synchronization and this instability continues even if the fault is cleared. An improper FL although it limits the frequency deviation but it still cannot save the converter from instability. A lower FL value can make the converter ride through the fault successfully and the lower FL, the less the transient peak phase.

Figure 8 shows the results in the situation of a voltage sag to 0.3 pu at 5 s and recovery at 5.1 s corresponding to the condition of no equilibrium point with $\Delta\dot{\omega}(t_0) < 0$. In this situation, the inclusion of the FL improves the synchronization stability. When $A_2+A_3 > A_1$, the phase of the converter without FL increases over than that with FL at t_3 and t_6. A small FL value can reduce the area of A_2+A_3 and make $A_2+A_3 < A_1$, then make the converter present a lower transient peak phase as shown by the cyan line in Fig. 8. On the other hand, as expected, the FL also limits the frequency deviation during the recovery so that it prolongs the settling time.

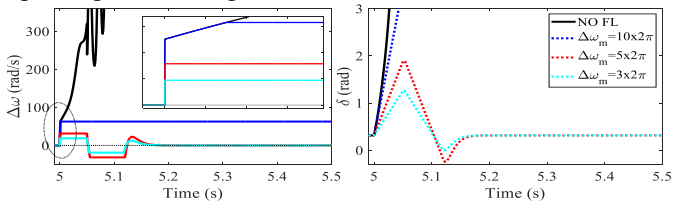

Fig. 7. Results in the situation of no equilibrium point with $\Delta\dot{\omega}(t_0) > 0$.

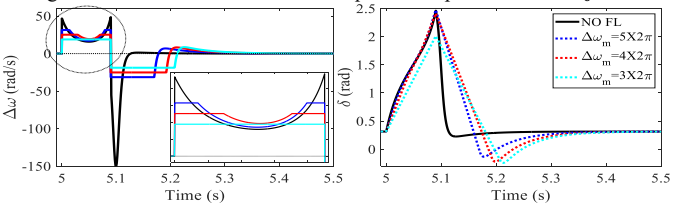

Fig. 8. Results in the situation of no equilibrium point with $\Delta\dot{\omega}(t_0) < 0$.

V. Conclusions

This letter analyses the mechanism of the synchronization stability caused by the frequency limiter in the PLL. The main conclusion of the letter is that the frequency limiter slows down the phase change but increases the settling time of the grid-feeding converter following a fault. Moreover, it is found that if an equilibrium point exists during the fault, FL degrades the synchronization stability by enlarging the transient peak phase; if no equilibrium point existed, the FL lowers the transient peak phase and extends the critical cleaning time. Anti-windup limiters can help alleviate the negative effect of the FL and further improve the synchronization stability. Future work will study the effect of different anti-windup strategies on the synchronization stability.

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