Impact of Frequency Anti-Windup Limiter on Synchronization Stability of Grid Feeding Converter

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***Abstract*—Loss of the synchronization is a one of the main issues for the grid-feeding converter in a weak grid after subjecting a large disturbance. The synchronous transient is highly nonlinear due to the phase movement and the frequency limiters. However, none of the previous research has considered the anti-windup PI in the phase-locked loop, which is commonly implemented in reality and introduced an additional nonlinear transient. This work provides a taxonomy to evaluate and compare the effect of different anti-windup PI limiters on the synchronization stability including the clamping, back-calculation and combined method. Different anti-windup PI limiters allocate zeros and poles differently and have different impacts on the damping and stability enhancement. A case study implemented in Matlab/Simulink serves to compare the trajectory of the converter phase and frequency using different anti-windup PI in the scenario of both with and without equilibrium point during the fault. Simulation results show that anti-windup PI limiters increase the damping during the fault and thus improve the synchronization stability margin.**

***Index Terms*—Synchronization Stability, Grid-Following Converter, Phase-Locked Loop (PLL), Frequency Limiter (FL).**

I. Introduction

A. Motivation

The grid-following converter (GFL) is a common interface used in the generation, transmission and distribution system [1]. While GFLs enable the integration of renewable energy resources, they also show issues, in particular concerning their synchronization with the grid. With this regard, the definitions of power system stability have been recently revised and extended to include the converter-driven stability [2]. Maintaining the synchronization with the grid is a basic requirement for the normal operation of the GFL, while in the presence of the fault, the GFLs should not disconnect from the grid but maintain a stable connection to avoid further contingencies [1]. However, in a weak grid, especially those with low short-circuit ratio (SCR) [3] and including lines with high R/X ratio [4], the GFL may lose its synchronization during a severe fault even if the fault ride through requirement is satisfied and this instability may continue even after the fault is cleared [5]. This synchronization instability related to the phase-locked loop (PLL) of the GFL has been identified as a particular issue of concern by the British transmission system operator (TSO) [6]. In this context, synchronization stability analysis has attracted considerable attention [7]. However, all recent works neglect the frequency limiter (FL) in the PLL, which is generally applied in the PLL control loop in practice to avoid an excessive frequency mismatch with the grid. There are several different possible implementations of PI control limiters, each of which has different dynamics and introduces an extra nonlinear element to the GFL synchronism. To the best of our knowledge, the impact of the different PI limiters on the synchronization transient response of GFLs as well as its stability has received scarce attention so far. This paper aims at filling this gap.

B. Literature Review

Synchronization stability of the converter is similar to the angle-rotor stability of the synchronous machine, which is defined as the ability of the grid-tied converter to maintain the synchronization after being subjected to a large disturbance [7]. In a strong grid, the grid impedance of which is negligible and the voltage at the point of common coupling (PCC) is assumed to be fixed, the synchronization stability solely depends on the PLL control loop [8]. While in a weak grid with non-negligible grid impedance, the PCC voltage couples to the grid injection from the GFL and this introduces a positive feedback to the synchronism resulting in the possibility of synchronization instability [9]. To represent the effect of this positive feedback on the synchronous transients, a 2nd-order Quasi-Static Large-Signal (QSLS) model has been proposed [9-11]. Although the QSLS model neglects the current transients which thus reduces its accuracy [12], the inclusion of the feed-forward compensator in the GFL can ensure an effective use of the QSLS model for synchronization stability analysis [13]. Based on this model, reference [14] illustrated the equivalence of the GFL synchronism to the electro-mechanism of the synchronous generator. Hence, the equal area criterion (EAC) method can be used for the stability analysis [15,16]. However, this method is applied under an assumption that the system is undamped, while the GFL presents a variable damping [3,17]. To enhance the assessment accuracy and estimate the stable region, the phase portrait [18,19] and Lyapunov Theorem [20-22] have been used.

The references above assume that the PI controller in the PLL is continuous without a limiter, while in the reality, to avoid a

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significant mismatch between the GFL and grid, FL is usually implemented. This FL is easily activated after a large disturbance. Our recent letter [23] considers such aspect and finds that the FL in the PLL degrades the synchronization stability if an equilibrium point exists during the fault, while it enhances if no equilibrium point existed. However, the work only considered a windup PI limiter, where the integrator keeps accumulating error during the frequency saturation resulting in a larger time elapsed until desaturation and a larger transient phase. Hence, in practice, the anti-windup PI limiter is necessary. The anti-windup PI limiter includes extra nonlinear dynamics and complicates the synchronization transients. Moreover, there are several different possible implementations of anti-windup PI limiter [24,25] and each of them can lead to substantially different dynamic responses [26]. For example, the clamping method based on a simple switch is recommended in the IEEE standard 421.5-2016 [27], and the back-calculation includes a feedback loop to discharge the integral accumulation [28]. An overview of modern anti-windup properties used in the GFL current control is given in [26,29]. However, no work before specifically analyzes the effect of the anti-windup PI limiters on the synchronization transients.

C. Contribution

Based on the QSLS model proposed in [9] and the taxonomy of PI limiters summarized in [26], this work provides a comprehensive analysis of the impact of the different PI limiters on the synchronization stability. The specific contribution of the paper are as follows.

1) To analyze the characteristics of the classical anti-windup PI limiters used in the PLL based on the transfer function.
2) To provide a taxonomic analysis of different PI limiters on the synchronization stability, especially on the dynamic trajectory of the GFL frequency and phase during both the fault and recovery.
3) To compare the effects of different anti-windup PI limiters with different settings on the synchronization stability.

D. Organization

The remainder of the paper is organized as follows. Section II reviews the taxonomy for the PI limiters and analyzes its impact on the synchronization stability based on the transfer functions. Section III analyzes the effects of the different anti-windup PI limiters on the synchronous dynamics in different scenarios. Section IV compares, by means of simulations, the performance of the different anti-windup PI limiters with different settings on the synchronization transients of the converters, while section V draws the conclusion.

II. PI Controllers In PLL

Figure 1 shows the structure of a typical GFL, where the GFL synchronizes with the grid at the point of common coupling (PCC) via the synchronous reference frame PLL (SRF-PLL). Assuming the PCC voltage is the reference with the phase at 0 rad, then the PCC voltage in the q-axis v_q or the input of the PI controller in the PLL can be obtained in (1).

$$v_q = r_g i_q^* + \omega l_g i_d^* - V_g \sin(\delta) \quad (1)$$

Where r_g is the grid resistance, l_g is the grid inductance, i_d^*, i_q^* are the current reference in the synchronous frame, V_g is the grid voltage, β is the output of the PI controller, ω is the GFL frequency, $\Delta\omega$ is the transient frequency deviation of the GFL to the grid frequency, δ is the phase difference between the GFL and grid, of which value equals to:

$$\frac{d\delta}{dt} = \Delta\omega \quad (2)$$

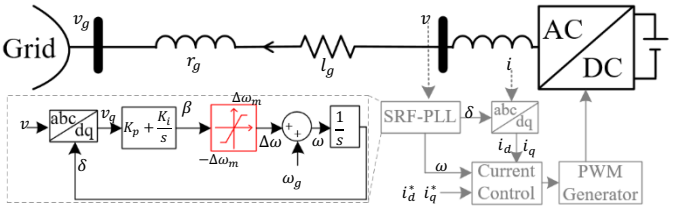


Fig. 1. Structure of a Grid-Following Converter

When the PLL achieves synchronization, the q-axis voltage (v_q) will be null in the fundamental frequency. As long as v_q is not zero, the integrator of the PI control accumulates the error. To restrict the error accumulated in the PI controller, and more importantly, to avoid an excessive frequency mismatch with the grid, a Frequency Limiter (FL) is normally implemented along with the PI controller in the SRF-PLL. Assuming the current control transient of the GFL is negligible with respect to the synchronization stability analysis [13], equation (1)(2) and the PI controller represents the synchronization transients of the GFL and defines the QSLS model as shown in Fig. 2.

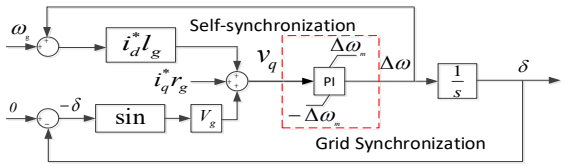


Fig. 2. Grid-Following Converter quasi-steady-state model

A. Taxonomy of PI limiters

There exist several implementations of PI control limiters, which changes the transient response of the SRF-PLL. This section provides a brief review on the various PI controllers as classified and summarized in Fig. 3.

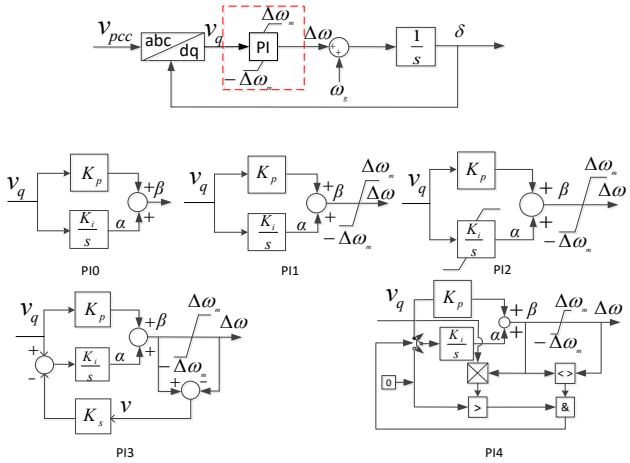


Fig. 3. Different PI limiter models

1) PI0: Linear Model

If no limiter is considered, the PI model is a simple linear model, as follows:

$$\dot{\alpha} = K_i v_q$$
$$\Delta\omega = K_p v_q + \alpha \quad (3)$$

where k_p and k_i are the PI coefficients; α is the integral output.

2) PI1: Windup Limiter

The limiter includes a nonlinear transient in the PI control. A windup limiter only limits the output β but leaves the integrator continuous as indicated follows:

$$\Delta\omega = \begin{cases} \Delta\omega_m & if \quad \beta > \Delta\omega_m \\ \beta & if \quad -\Delta\omega_m < \beta < \Delta\omega_m \\ -\Delta\omega_m & if \quad \beta < -\Delta\omega_m \end{cases}$$
$$\dot{\alpha}_{PI1} = K_i v_q$$
$$\beta = K_p v_q + \alpha \quad (4)$$

where $\Delta\omega_m$ is the limited value, β is the unsaturated PI controller output. During the saturation, the error is accumulated in the integrator and the output β keeps rising, resulting in a difficulty on desaturation.

3) PI2: Anti-Windup Limiter (Clamping)

The purpose of the anti-windup method is to avoid the accumulation in the integral by modifying the value of $\dot{\alpha}$ when the control output is saturated. Clamping or conditional integration is a widely used anti-windup method, especially in case of digital control systems, e.g. IEEE Standard 421.5-2016, which uses a simple switch to set the integral path $\dot{\alpha}$ to be zero.

$$\dot{\alpha}_{PI2} = \begin{cases} 0 & if \ \ \beta - \Delta\omega_m \neq 0 \\ K_i v_q & otherwise \end{cases} \quad (5)$$

Note that the integrator holds its value after the limitation reached but it does not reset. Consequently, during the desaturation, it still needs to discharge the integral accumulation.

4) PI3: Anti-Windup Limiter (Back-Calculation)

The back-calculation (or tracking anti-windup or anti-reset) windup method utilizes the difference between the limiter input and output as feedback to reduce the integral accumulation by modifying the expression of $\dot{\alpha}$ as follows:

$$\dot{\alpha}_{PI3} = K_i v_q - K_s K_i (\beta - \Delta\omega_m) \quad (6)$$

Where k_s is the back-calculation coefficient in the feedback to counteract the error into the integrator and even discharge the integrator if $|K_s K_i(\beta - \Delta\omega_m)| > |K_i v_q|$.

This gain determines the performance of anti-windup; a proper coefficient enables a better performance than the clamping, while an improper coefficient leads to worse results with no improvement at all.

5) PI4: Anti-Windup Limiter (Combined Clamping and Back-Calculation)

Combined clamping and back-calculation method combines the advantages of both methods. This is obtained with the following logic:

$$\dot{\alpha}_{PI4} = \begin{cases} -K_s K_i(\beta - \Delta\omega_m) & if \ \ \beta - \Delta\omega \neq 0 \ and \ v_q\beta > 0 \\ K_i v_q & otherwise \end{cases} \quad (7)$$

In comparison with (5) and (6), if K_s is small and approaches to zero, then the clamping function becomes dominant; while if K_s is large, then the back-calculation function becomes dominant.

The clamping method blocks the error of the integral while the back-calculation method reduces the input that contributes to the integral. If K_s is small, then $|\dot{\alpha}_{PI4}| < |\dot{\alpha}_{PI2}| = 0 \leq |\dot{\alpha}_{P3}| \leq |\dot{\alpha}_{P1}|$; while if K_s is large, then $|\dot{\alpha}_{PI4}| < |\dot{\alpha}_{PI3}| \leq |\dot{\alpha}_{P2}| = 0 \leq |\dot{\alpha}_{P1}|$. Since PI4 combines clamping and back-calculation, it is expected to show the best performing anti-windup behavior.

Besides those outlined above, there are many other anti-windup methods based on extensions from PI2~PI4. The above methods are classical and are sufficient to represent the sensitive characteristics of all the others, therefore, the theoretical analysis in this paper is based on these models.

B. Transfer function analysis of different PI limiters

When the frequency is within the limits, the PLL shows a linear PI dynamic response, the characteristics of which have been well discussed in the literature [3,17,30]. The interest of this paper is to analyze and compare the PLL dynamics using different PI limiters (PI1~PI4) during the frequency saturation. The damping effect is one of the critical impacts on the synchronous transients, which can be intuitively analyzed by the transfer function.

The FL breaks the PLL closed-control loop: after the FL, the dynamics from the phase movement and further PCC voltage are identical for PI1~PI4; before the FL, the dynamics from the v_q to β are different depending on their own technique. The dynamics of β dominate the process of the desaturation and then the GFL response. Figure 4 shows the transfer functions of PI1~PI4 under the condition that the frequency is saturated at $\Delta\omega_m$, where G_{gfl} represents the transfer function from $\Delta\omega_m$ to v_q.

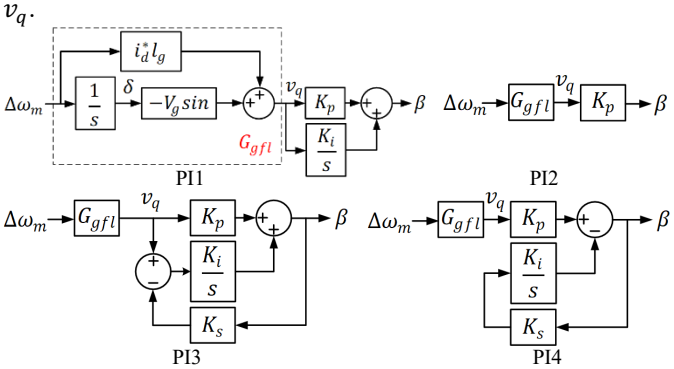


Fig. 4. Transfer function of the PI limiters

In Fig. 4, except for PI2 which 1st order, all others are of the 2nd order. For a fair comparison, all the transfer functions of PI1~PI4 are written in the format of a standard second order (8) and Table I compares their specific corresponding elements.

$$G_{PI\{\blacksquare\}}(s) = \frac{K(s - z_1)(s - z_2)}{(s - p_1)(s - p_2)} \quad (8)$$

TABLE I
COMPARISON OF THE TRANSFER FUNCTION OF DIFFERENT PI LIMITERS

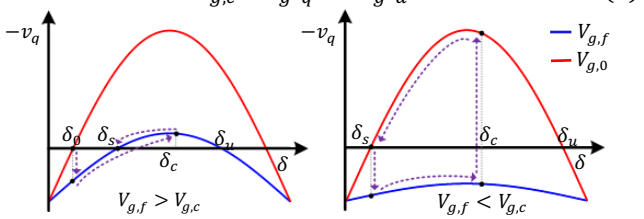
PI limiter	PI1	PI2	PI3	PI4
K	$l_g i_d^* K_p$	$l_g i_d^* K_p$	$l_g i_d^* K_p$	$l_g i_d^* K_p$
z_1	$V_g/i_d^*/L_g$	$V_g/i_d^*/L_g$	$V_g/i_d^*/L_g$	$V_g/i_d^*/L_g$
z_2	$-K_i/K_p$	0	$-K_i/K_p$	0
p_1	0	0	0	0
p_2	0	0	$-K_i K_s$	$-K_i K_s$

Table I shows that K, z_1, p_1 are identical for PI1~PI4. The windup limiter PI1 has two poles at zero and presents a -2dB/decade slope. The clamping method PI2 and PI4 allocates a zero to the original in order to cancel a pole and make its transfer function become 1st order slowing down the increase in β. The back-calculation method PI3 and PI4 allocates the pole from the original to $-K_i K_s$ slowing down the increase in β. The larger K_s, the larger the damping and the better the stability. Especially for PI4, one of its poles has been cancelled by the clamping part and another has been moved towards the lefthand side of the imaginary axis by the back-calculation part. Note that while the discussion so far has considered a linearized transfer function, the study of the GFL synchronization stability is carried out in the remainder of this paper as well as in the case study considering large perturbations and the fully-fledged nonlinear transient response of the converters.

III. TAXONOMY OF PLL FREQUENCY PI-CONTROLLERS LIMITER IMPACT

After the occurrence of a fault and depending on its severity, GFL can show different dynamic responses. Figure 5 shows the trajectory of $-v_q$ vs. phase angle δ for the pre-fault ($V_{g,0}$) and fault ($V_{g,f}$) grid voltage levels. In the scenario of a mild fault where the equilibrium point of the GFL still exists, the GFL would tend to converge to the stable point. While in the scenario of a severe fault where the equilibrium point disappears, the GFL would keep accelerating and become unstable if the fault is not cleared in time. Thus, the analysis of the dynamic response of the GFL shall be classified according to the existence of the equilibrium point during the fault, where the critical fault voltage $V_{g,c}$ can be easily computed from (1).

$$V_{g,c} = r_g i_q^* + \omega l_g i_d^* \quad (9)$$



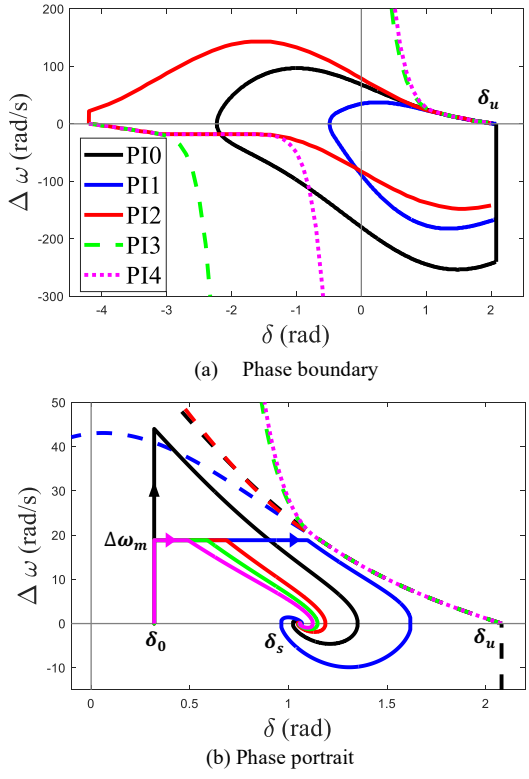
(a) Equilibrium Point exists (b) Equilibrium point does not exist

Fig. 5. Classification of the synchronization stability with the fault scenarios

A. Scenario 1: Equilibrium point existence

In this scenario, the grid voltage sags, but its magnitude remains above $V_{g,c}$, i.e. $V_{g,f} \in [V_{g,c}\ V_{g,0})$. There are two equilibrium points with a stable one at $\delta_s = \sin^{-1}\frac{r_g i_q^* + \omega_g l_g i_d^*}{V_{g,f}}$ and an unstable one at $\delta_u = \pi - \sin^{-1}\frac{r_g i_q^* + \omega_g l_g i_d^*}{V_{g,f}}$. After the fault, GFL accelerates with $\Delta\omega > 0$ and the phase increases. As long as $\Delta\omega$ decelerates to 0 before the peak phase δ_c exceeds δ_u, the GFL will be stable and its phase will move back to δ_s. In other words, δ_u is a critical point at the stability boundary. Based on the converter parameter used in the case studies in Section IV, the stability boundary in the phase portrait as shown in Fig. 6 (a) can be obtained by the means of the inversely time integral of the PI0~PI4 from the unstable equilibrium point at $V_{g,c} = 0.36\,pu$ with $\delta_u = 2.08\,rad$. The area of the upper stability region in a descending order is: PI4, PI3, PI2, PI0, PI1. Note, this paper we are not specifically doing the analysis on the stability boundary. Fig. 6 (b) shows the process of the phase moving from δ_0 to δ_s during the fault, where the dotted line represents the corresponding stability boundary, which encircles a stable movement of the GFL. Since the PLL only experiences a normal PI during the desaturated frequency dropping from $\Delta\omega_m$ to 0, the stability boundaries for all the PI controller are identical. Hence, the phase at the limited frequency can be used to evaluate the PI effects on the synchronization stability, which refers to the critical time $t_{PI\{\blacksquare\}}$ at $\beta_{PI\{\blacksquare\}}(t_{PI\{\blacksquare\}}) = \Delta\omega_m$ in the time-domain diagram (see Fig. 7) that the shorter $t_{PI\{\blacksquare\}}$ the better the stability margin.

Note that in Fig. 6 and later in Fig. 8 we purposely set a large K_s to ensure the discharge of the integrator from the back-calculation loop, i.e. $|K_s K_i(\beta - \Delta\omega_m)| > |K_i v_q|$, in this case, as indicated in (6) and (7), the larger the β, the larger the back-calculation and the quicker the desaturation. Hence, PI3 and PI4 presents no boundary on the frequency deviation.



(a) Phase boundary

(b) Phase portrait

Fig. 6. PI0~PI6 phase portrait in the scenario of equilibrium point existence

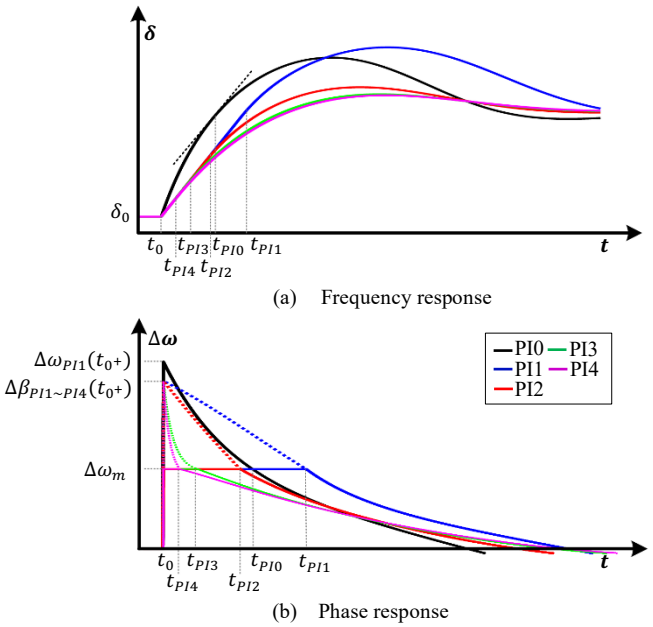


Fig. 7. PI0~PI6 dynamics in the scenario of equilibrium point existence

1) PI0: No FL

Initially, the PLL works as the normal PI process with $V_g = V_{g,0}$ and the phase δ_0 less than 90°. At the instant of the grid voltage sag to $V_{g,f}$, only the proportional channel of the PI controller activates in Fig. 2. If the frequency is unlimited, i.e. PI0, then $\Delta\omega$ and v_q at t_{0^+} would be:

$$\Delta\omega_{PI0}(t_{0^+}) = \frac{K_p(V_{g,0} - V_{g,f})\sin\delta_0}{1 - K_p l_g i_d^*} \quad (10)$$

$$v_{PI0,q}(t_{0^+}) = l_g i_d^* \Delta\omega_{PI0}(t_{0^+}) + (V_{g,0} - V_{g,f})\sin\delta_0 \quad (11)$$

Where $v_{PI0,q}(t_{0^+})$ and $\Delta\omega_{PI0}(t_{0^+})$ both are positive values. As the fault continues, the GFL dynamics would be:

$$v_{PI0,q}(t) = l_g i_d^* \Delta\omega_{PI0}(t) + V_{g,0}\sin\delta_0 - V_{g,f}\sin(\delta_0 + \int_{t_0}^{t}\Delta\omega_{PI0}(t)dt) \quad (12)$$

$$\Delta\omega_{PI0}(t) = \beta_{PI0}(t) = K_p v_{PI0,q}(t) + K_i\int_{t_0}^{t} v_{PI0,q}(t)\,dt \quad (13)$$

Defining the time t_{PI0} as the time it takes for $\beta_{PI0}(t)$ to become less than $\Delta\omega_m$, i.e. $t_{PI0} = \{t_{PI0} | t_{PI0} \in N^+, \beta_{PI0}(t_{PI0}) = \Delta\omega_m\}$. Since $v_{PI0,q}(t)$ is positive in the period of $\beta_{PI0}(t)$ decelerating to $\Delta\omega_m$, the larger K_i the larger t_{PI0} and the worse the synchronization stability.

2) PI1: Windup Limiter

When $\Delta\omega_{PI0}(t_{0^+}) > \Delta\omega_m$, PI1 limits its output at $\Delta\omega_m$. The feedback of the self-synchronization loop in Fig. 2 is limited and then for PI1~PI4 the unlimited frequency β_{PI1}~β_{PI4} at t_{0^+} would be equal and can be computed as:

$$\beta_{PI1}(t_{0^+}) = K_p(\Delta\omega_m l_g i_d^* + (V_{g,0} - V_{g,f})\sin\delta_0) \quad (14)$$

Comparing (14) with (10), due to $\Delta\omega_{PI0}(t_{0^+}) > \Delta\omega_m$, it can be obtained that $\Delta\omega_{PI0}(t_{0^+}) > \beta_{PI1}(t_{0^+}) > \Delta\omega_m$. Since PI1 is in windup, with the integrator accumulating the error during the saturation then β_{PI1} would be:

$$v_{PI1,q}(t) = l_g i_d^* \Delta\omega_m + (V_{g,0} - V_{g,f}\cos(\Delta\omega_m t))\sin\delta_0 - V_{g,f}\cos\delta_0\sin(\Delta\omega_m t) \quad (15)$$

$$\beta_{PI1}(t) = K_p v_{PI1,q}(t) + K_i\int_{t_0}^{t} v_{PI1,q}(t)dt \quad (16)$$

When $\beta_{PI1}(t)$ becomes lower than $\Delta\omega_m$ at t_{PI1}, i.e. $t_{PI1} = \{t_{PI1} | t_{PI1} \in N^+, \beta_{PI1}(t_{PI1}) = \Delta\omega_m\}$, the PI1 withdraws the saturation. During the saturation, since PI0 inputs a larger error than PI1, i.e. $v_{PI0,q} > v_{PI1,q}$, then after experiencing the same PI dynamics, PI0 stabilizes faster than PI1, i.e. $t_{PI0} < t_{PI1}$ as shown in Fig. 7. Therefore, the windup limiter worsens the synchronization stability.

3) PI2: Anti-windup Limiter (Clamping)

In PI2, as long as $\beta_{PI2}(t) > \Delta\omega_m$, the integral part is switched off and the PLL works in the first-order mode (17) until $t_{PI2} = \{t_{PI2} | t_{PI2} \in N^+, \beta_{PI2}(t_{PI2}) = k_p v_{PI2,q}(t_{PI2}) = \Delta\omega_m\}$. Since the error is identical ($v_{PI2,q}(t) = v_{PI1,q}(t)$) and $\beta_{PI2}(t) < \beta_{PI1}(t)$, PI2 desaturates faster than PI1, i.e. $t_{PI2} < t_{PI1}$ as shown in Fig. 7.

$$\beta_{PI2}(t) = K_p v_{PI2,q}(t) \quad (17)$$

When $\beta_{PI2}(t)$ becomes lower than $\Delta\omega_m$, the integral channel is connected again and starts to accumulate the error. Normally, K_i is small and PI2 will work as a general PI process. t_{PI2} is independent of K_i. However, if K_i is very large and resulting in the error accumulation in the I-control being faster than its reduction in the P-control, i.e. $K_p v_{PI2,q}(t_{PI2} + \Delta t) < K_i\int_0^{\Delta t} v_{PI2,q}(t)dt$, then PI2 will be saturated again and $\beta_{PI2}(t)$ will swing between the saturation and $K_p v_{PI2,q}(t)$, until the time t'_{PI2} that the decrease in P-control becomes dominant, i.e. $K_p v_{PI2,q}(t'_{PI2}) + K_i\int_{t_{PI2}}^{t'_{PI2}} v_{PI2,q}(t)dt = \Delta\omega_m$. Note, $t_{PI2} < t'_{PI2} < t_{PI1}$.

4) PI3: Anti-Windup Limiter (Back-Calculation)

PI3 uses the exceeded frequency ($\beta_{PI3}(t) - \Delta\omega_m$) to lower the error input in the integral channel during the saturation. Hence, its anti-windup performance depends on K_s.

$$\beta_{PI3}(t) = K_p v_{PI3,q}(t) + K_i\int_{t_0}^{t}(v_{PI3,q}(t) - K_s(\beta_3(t) - \Delta\omega_m))dt \quad (18)$$

If K_s approaches zero, due to $v_{PI3,q}(t) = v_{PI1,q}(t)$, then it has a similar performance with PI1 as can be seen from a comparison between (18) and (13); If K_s approaches $v_{PI3,q}(t)/(\beta_{PI3}(t) - \Delta\omega_m)$, then it has a similar performance with PI2 since K_s exactly cancels the integral accumulation; if K_s is greater than $v_{PI3,q}(t)/(\beta_3(t) - \Delta\omega_m)$ and approaching to infinity, K_s turns the integrator to be negative and speeds the desaturation. Regardless of the numerical issue, $\lim_{t\to t_{0^+}} \beta_{PI3}(t)$ can be reduced to $\Delta\omega_m$. Thus, $t_{PI3} < t_{PI2}$ as shown in Fig. 7.

5) PI4: Anti-Windup Limiter (Combined Clamping and Back-Calculation)

The combined method PI4 on the one hand blocks the error

input to the integral and on another hand feeds the exceeded frequency into the integral to lower the value from the proportional channel.

$$\beta_{PI4}(t) = K_p v_{PI4,q}(t) - K_i \int_{t_0}^{t} (K_s(\beta_{PI4}(t) - \Delta\omega_m))dt \quad (19)$$

Thus, even K_s approaches to zero, PI4 has a similar performance with PI2 but not PI1. With K_s increasing, PI4's performance would be similar with PI3, but its value of $\beta_{PI4}(t)$ is lower, about $K_i \int_{t_0}^{t} v_{PI3,q}(t)\,dt$, as can be seen by comparing (19) and (18). Thus, $t_{PI4} < t_{PI3}$ as shown in Fig. 7.

Since the integral part $-K_i \int_{t_0}^{t_{PI4}} (K_s(\beta_{PI4}(t) - \Delta\omega_m))dt$ is less than zero at the instant of the withdrawal of the limitation, then unlike PI2, PI4 will not swing but directly go into the normal PI process.

B. Scenario 2: No Equilibrium Point

In this scenario, the grid voltage sags below $V_{g,c}$, i.e. $V_{g,f} \in [0\ V_{g,c})$. There is no equilibrium point. As shown in Fig. 5, $v_q < 0$ all the time during the fault, the GFL keep accelerating. Then during the fault PI1-PI4 has the same performance as shown in Fig. 9, while PI0 presents a quick increase in the phase and in the frequency. However, after the fault clearance, since PI1-PI4 use different techniques on the PI controller, their responses during the recovery would be different and this raises the question whether their operating point can move back to the stable point. Fig. 8 (a) shows the stability boundaries of the PI0-PI4 at the post-fault with $\delta_u = 2.82\ rad$, where the area of the upper stability region in a descending order is: PI3, PI4, PI0, PI2, PI1. Fig. 8 (b) shows the process of the phase moving from δ_s to δ_c at the instant of the fault clearance and back to δ_s after, where the dashed line represents the corresponding stability boundary and the dotted line represents the $\beta(\delta)$. When the fault cleaning angle δ_c closes to δ_u, for a stable trajectory after the fault clearance, GFL has to decelerate ($\Delta\omega < 0$). Since the fault cleaning angle for PI1-PI4 at the same fault cleaning time t_c would be identical, frequency $\beta_{PI\{\blacksquare\}}$ at the fault cleaning time ($\Delta\omega_{PI\{\blacksquare\}}(t_c)$) can be used to evaluate the effects of different PI controllers on the synchronization stability that the negatively larger $\beta_{PI\{\blacksquare\}}$ the better the stability margin.

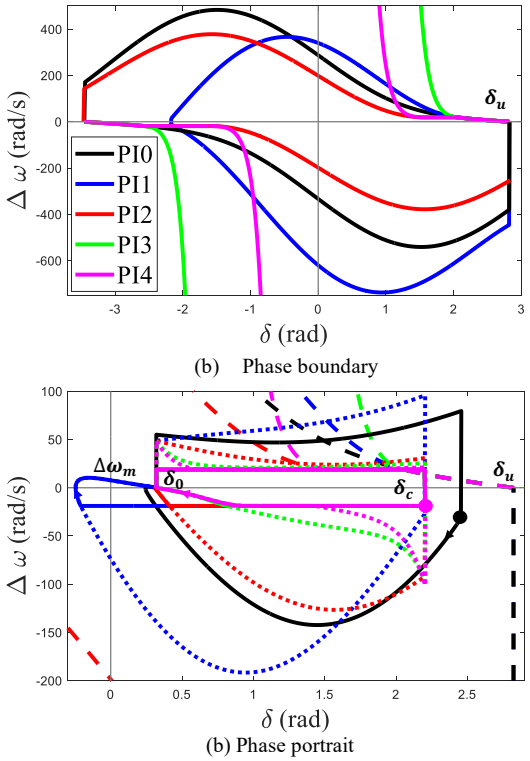
1) PI0: No FL

Assuming that the fault is cleared at t_c, the frequency of PI0 would instantly change to be:

$$v_{PI0,q}(t_c{+}) = l_g i_d^* \Delta\omega_0(t_c) + V_{g,0}\sin(\delta_0) - V_{g,0}\sin\left(\delta_0 + \int_{t_0}^{t_c} \Delta\omega_{PI0,q}(t)dt\right) \quad (20)$$

$$\beta_{PI0}(t_c{+}) = \Delta\omega_{PI0}(t_c) = K_p v_{PI0,q}(t_c) + K_i \int_{t_0}^{t_c} v_{PI0,q}(t)dt \quad (21)$$

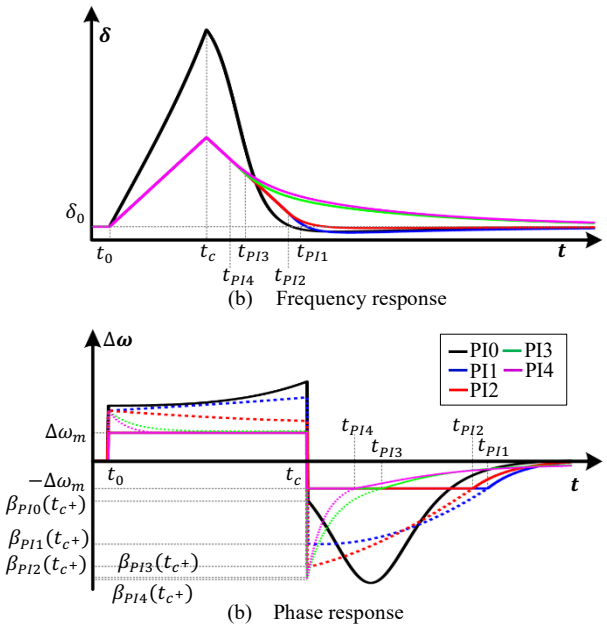
After the fault clearance, for a stable operation, $v_{PI0,q}(t_c)$ must be negative to reduce the $\omega_{PI0}(t)$ and enforce the phase moving back.



(b) Phase boundary

(b) Phase portrait

Fig. 8. PI0~PI6 phase portrait in the scenario of no equilibrium point



(b) Frequency response

(b) Phase response

Fig. 9. PI0~PI6 dynamics in the scenario of no equilibrium point

2) PI1: Windup Limiter

Although $\Delta\omega_{PI1}(t)$ is bounded by the limiter, the lack of an anti-windup mechanism results in $\beta_{PI1}(t)$ increasing during the fault. At the instant of the fault clearance, the voltage becomes:

$$v_{PI1,q}(t_c{+}) = -l_g i_d^* \Delta\omega_m + V_{g,0}\sin(\delta_0) - V_{g,0}\sin(\delta_0 + \Delta\omega_m t_c) \quad (22)$$

Since $\delta_u > (\delta_0 + \Delta\omega_m t_c) > \delta_0$ and $t_c < \frac{\delta_u - \delta_0}{\Delta\omega_m}$ for a stable

operation, t_c would be very small and $\left|K_p v_{PI1,q}(t_c{+})\right| > K_i \int_{t_0}^{t_c} v_{PI1,q}(t)dt$. Then, $\beta_{PI1,q}(t_c{+}) \ll 0$ and $\Delta\omega_{PI1,q}(t)$ turns to be inversely saturated at $-\Delta\omega_m$. Therefore, after fault clearance, the phase linearly decreases at the rate of $-\Delta\omega_m$, and the q-axis voltage negatively decrease approaching to zero. Until $t_{PI1} = \{t_{PI1} | \, t_{PI1} \in N^+, \beta_{PI1}(t_c + t_{PI1}) = -\Delta\omega_m\}$, PI1 returns to work as the normal PI process.

Since $\int_{t_0}^{t_c} \Delta\omega_{PI0,q}(t)dt > \Delta\omega_m t_c$ that the error accumulated in PI0 is greater than that in PI1, then $\beta_{PI1,q}(t_c{+}) < \beta_{PI0,q}(t_c{+})$ and PI1 presents a higher stability.

3) PI2: Anti-windup Limiter (Clamping)

At the instant of the fault clearance, PI2 presents the same phase as PI1 i.e. $v_{PI2,q}(t_c{+}) = v_{PI1,q}(t_c{+})$. However, on the one hand, since the integral of the PI2 did not positively accumulate the error during the fault, $\beta_{PI2}(t_c{+}) < \beta_{PI1}(t_c{+})$ and thus PI2 presents a higher stability than PI1; on the other hand, since after the fault clearance the frequency is saturated, PI2 still works on the 1st-order as indicated in (23) so that it desaturates faster as shown in Fig. 9, i.e. $t_{PI2} < t_{PI1}$. Note, before t_{PI2}, PI2 presents an exact performance similar to PI1 in terms of voltage and phase.

$$\beta_{PI2}(t_c + t) = K_p v_{PI2,q}(t_c + t) \tag{23}$$

4) PI3: Anti-Windup Limiter (Back-Calculation)

As explained before, the performance of the PI3 depends on its back-calculation coefficient K_s. Referring to (18), after the fault clearance, the frequency β_{PI3} would be as (24):

$$\begin{aligned}\beta_{PI3}(t_c + t) &= K_p v_{PI3,q}(t_c + t) \\ &+K_i \int_{t_0}^{t_{ccr}} \left(v_{PI3,q}(t) - K_s(\beta_{PI3}(t_c) - \Delta\omega_m)\right) dt \\ &+K_i \int_{t_c}^{t} (v_{PI3,q}(t_c + t) - K_s(\beta_{PI3}(t_c + t) + \Delta\omega_m))\, dt\end{aligned} \tag{24}$$

The larger K_s, the larger the damping. During the fault, PI3 slows down the phase change, thus enhancing stability, while during the recovery, it slows down the phase moving back to the initial value.

During the fault, $v_{PI3,q}(t)$ is positive and the back-calculation loop introduces a negative value to lower the integral; while during the recovery, $v_q(t)$ is negative and back-calculation loop introduces a positive value to increase the integral. When K_s approaches to $v_{PI3,q}(t_c + t)/(\beta_{PI3}(t_c + t) + \Delta\omega_m)$, PI3 has a similar response with PI2 during the recovery. Since $\frac{v_{PI3,q}(t_c+t)}{\beta_{PI3}(t_c+t)+\Delta\omega_m} < \frac{v_{PI3,q}(t)}{\beta_3(t)-\Delta\omega_m}$, if PI3 is adjusted to have the same performance as PI2 during the fault, then its settling time would be longer during the recovery.

5) PI4: Anti-Windup Limiter (Combined Clamping and Back-Calculation)

PI4 has the best anti-windup ability amongst PI2-PI4. If there is an equilibrium point during the fault, PI4 can help slow down the phase movement and improve the stability. While during the recovery process in the scenario of the non-equilibrium point, PI4 presents a higher value than PI3 in the integral for the same K_s, thus, it behaves a stronger damping than PI3 and prolongs the settling time as shown in Fig. 9.

$$\begin{aligned}\beta_{PI4}(t_c) &= K_p v_{PI4,q}(t_c) \\ &-K_i K_s \int_{t_0}^{t_c} (\beta_{PI4}(t_c) - \Delta\omega_m)\, dt\end{aligned} \tag{25}$$

During the fault, PI4 accumulates negative errors in its integral so that $\beta_{PI4}(t_c) < \beta_{PI1}(t_c)$ and $\beta_{PI4}(t_c) < \beta_{PI3}(t_c)$ in comparison (25) with (22) and (24). Therefore, although PI4 may stabilize more slowly, it would have the best performance amongst all the PI limiters.

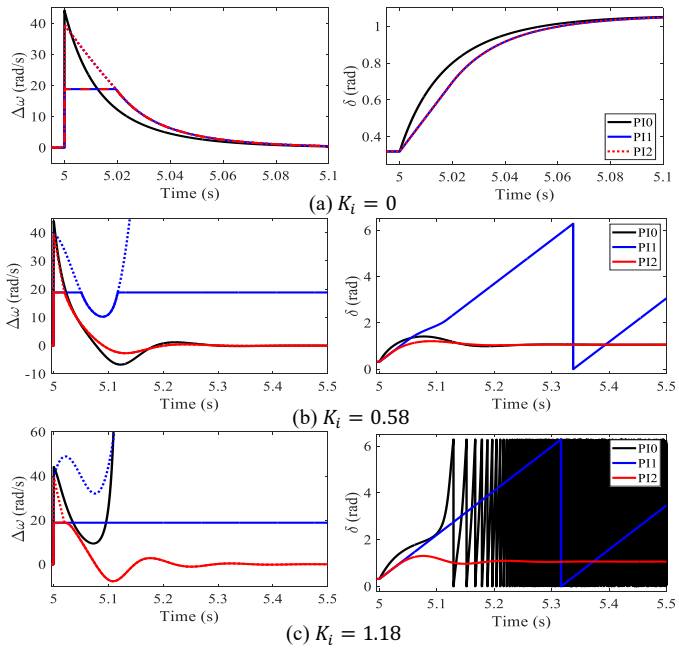
IV. Case Study

A time-domain EMT simulation solved in Matlab/Simulink serves to verify the comparative analysis on the impact of different anti-wind PI limiters on the synchronization stability. A 10 kV, 1 MW grid-feeding converter connected to a 50 Hz grid through an 0.38 pu L-filter and an $l_g = 0.31\ pu$, $r_g = 0.01\ pu$ grid impedance is discussed as shown in Fig. 1. The converter setpoint is $i_q^* = 0.95\ pu$; $i_q^* = 0.4\ pu$. The PLL frequency is limited in a range of 50 ± 3 Hz, $\Delta\omega_m = \pm 6\pi$ rad/s and its basic PI parameters K_p/K_i are 0.022/0.392 pu. The feed-forward compensator of the PCC voltage is implemented in the converter current control, for which the PI parameters are 12/2.4 pu. The critical grid voltage that the existence of a post-fault equilibrium point is $V_{g,c} = 0.31\ pu$. There are two scenarios under the consideration corresponding to existence of the equilibrium point during the fault.

A. Scenario 1

This scenario considers the grid voltage sag $V_{g,f}$ to be 0.36 pu at 5 s. The initial phase δ_0 is 0.32 rad. After the fault occurrence, there are two equilibrium point with $\delta_s = 1.06$ rad and $\delta_u = 2.08$ rad.

Figure 10 compares the transient response of the PLL using PI0~PI2 with different values of the K_i coefficient, where the dashed line in the figure of $\Delta\omega$ presents $\beta_{PI\{\blacksquare\}}$. In the case of a low K_i or even no integral part as shown in Fig. 10(a), the PLL works as the 1st order process and the mechanism of PI1 would be equivalent to that of PI2. Because the error feedback is limited by the FL, PI0 stabilizes faster than PI1 and PI2. With K_i increasing as shown in Fig.10(b), as expected, PI1 desaturates slower than PI0 and because of this, β_{PI2} fail to decrease to zero before its phase exceeds δ_u thus resulting in the loss of synchronization. In the case of a large K_i as shown in Fig.10(c), PI0 loses synchronization stability due to a significant error accumulated in the integral increasing β_{PI1}. Due to no error accumulating in PI2, it can stabilize at δ_s irrespective of the value of K_i. Since the frequency of PI2 is limited from the instant of the fault occurrence, its desaturation process in all the K_i cases are identical. It is noticed that in the case of $K_i = 1.18$, because $K_p v_{PI2,q}(t_{PI2} + \Delta t)$ is less than $K_i \int_0^{\Delta t} v_{PI2,q}(t)dt$, β_{PI2} swings around $\Delta\omega$ and prolongs the desaturation time from t_{PI2} to t'_{PI2} in comparison with other cases.



(a) $K_i = 0$

(b) $K_i = 0.58$

(c) $K_i = 1.18$

Fig. 10. PI0~PI2 comparison in Scenario 1 with K_i increasing

Figure 11 compares the transient response of the PLL using PI1~PI3 for different values of K_s coefficient. At the instant of the fault, $\beta_{PI\{\blacksquare\}}(t_0^+)$ is identical for the PI with FL. As expected, the performance of PI3 depends on K_s. If $K_s = 0$, PI3 loses the back-calculation loop and its mechanism fundamentally is similar with PI1. By the means of tuning K_s to cancel the error input, PI3 could have the same performance as PI2. A larger K_s can help desaturate even from the beginning of the saturation as the green line in Fig. 10, thus it improves the stability.

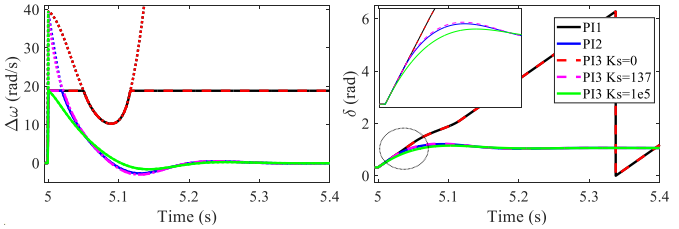


Fig. 11. PI1~PI3 comparison in Scenario 1 with K_s increasing

Figure 12 compares the transient response of the PLL using PI3~PI4 for different values of K_s coefficient. PI4 can avoid the instability from the error accumulating in the integral during the saturation so that it presents a better performance in the case of a low K_s and a quick desaturation in the case of a mild K_s. Of course, if K_s is large enough and the back-calculation becomes dominant, PI4 would have a similar performance with PI3.

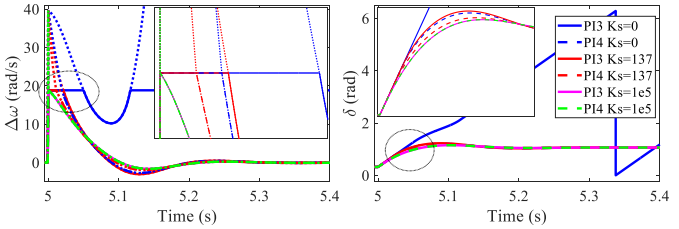


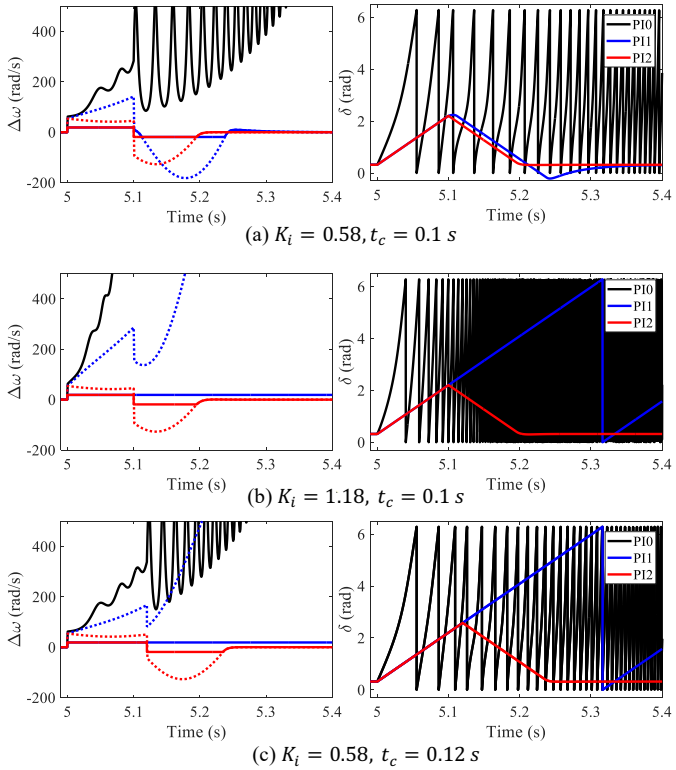
Fig. 12. PI3~PI4 comparison in Scenario 1 K_s increasing

B. Scenario 2

This scenario considers the grid voltage sag $V_{g,f}$ to 0.15 pu at 5 s. The initial phase δ_0 is 0.32 rad. After the fault occurrence, there is no equilibrium point.

Figure 13 compares the transient response of the PLL using PI0~PI2 under different K_i coefficients and fault cleaning times t_c. In this scenario, PI1 has a better synchronization stability than PI0 in that the FL restricts the phase and further increasing of $\beta_{PI\{\blacksquare\}}$ as shown in Fig. 13(a). Thus, after the fault clearance, β_{PI1} turns to be negative decelerating the GFL while $\Delta\omega_{PI0}$ is still positive resulting in the loss of synchronization. PI1 has the windup limiter and the error accumulation in the integral is related to the K_i coefficient and the cleaning time t_c. Hence, the higher K_i coefficient, the longer cleaning time t_c, the lower synchronization stability. Due to the switch-off of the integral during the saturation, the dynamic response of the PI2 is insensitive to the K_i coefficient as shown in Fig. 13(b). Moreover, β_{PI2} is only a sinusoidal function of phase that decreases during the fault. This make PI2 tolerate a longer fault cleaning time as shown in Fig. 13(c).

Figure 14 compares the transient response of the PLL using PI2 and PI3 for different values of K_s coefficient. In this scenario, when K_s is tuned to present the same response during the fault, it presents a higher damping and quick desaturation during the recovery. As expected, the increase in K_s negatively increases $\beta_{PI3}(t_c^+)$ and enhances synchronization stability but this action also increases the GFL damping and prolongs the settling time. Particularly, when K_s is large enough, PI3 can instantly desaturate at the instant of both fault occurrence and clearance.



(a) $K_i = 0.58, t_c = 0.1\ s$

(b) $K_i = 1.18,\ t_c = 0.1\ s$

(c) $K_i = 0.58,\ t_c = 0.12\ s$

Fig. 13. Comparison of PI1~PI3 in Scenario 2 with different K_i and t_c

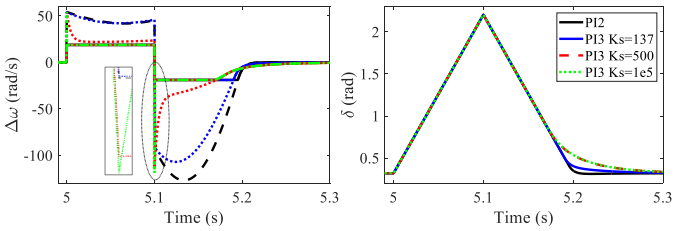


Fig. 14. Comparison of PI2 and PI3 in Scenario 2 with different K_s

Figure 15 compares the transient response of the PLL using PI3 and PI4 for different values of K_s coefficient. PI4 desaturates faster than PI3 so that at the instant of the fault clearance, it has a lower $\beta(t_c^+)$ but presents a higher damping after.

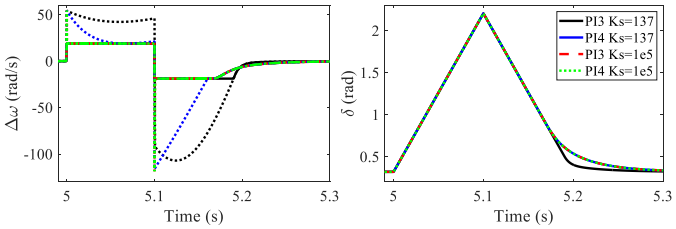


Fig. 15. Comparison of PI3 and PI4 in Scenario 2 with different K_s

V. Conclusions

This paper analyses and compares the mechanism of the synchronization stability caused by the different frequency limiters in the PLL. The main conclusion can be drawn as follows:

1) The windup limiter supresses the phase change in the GFL. This action enlarges the error feeding back into the PLL during the deceleration. In scenarios for which the equilibrium point exists, this deceleration leads to a slower PLL frequency stabilization and reduces the stability margin. On the other hand, for scenarios for which no equilibrium point exists, the windup limiter reduces the error feeding into the PLL during the acceleration. This leads to a lower frequency change and to a higher stability margin.
2) The clamping method removes a pole at the origin, whereas the back-calculation moves this pole negative. These actions increase the damping of the GFL and reduce the change rate of the PLL integral channel $\dot{\alpha}$, thus resulting in a short peak phase δ_c and a large motion back to the stable equilibrium point. Both the clamping and the back-calculation methods thus, have the effect to improve the synchronization stability margin.
3) The dynamics of the clamping method is mainly related to the fault clearing time, whereas that of the back-calculation is related to the K_s coefficient. The larger the K_s value, the larger the damping and the faster the desaturation. The effect of the K_s value is thus to reduce the settling time in the scenarios for which the equilibrium point exists, and to increase the settling time in the other scenarios.

An interesting consequence of the effect of anti-windup limiters, namely, the increase of the damping is that it makes the equal area criterion not reliable to determine the stability of GFLs. The stability assessment of GFL becomes thus more involved if anti-windup limiters are included. The authors aim at solving this issue in future works.

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